FullFlex™ Synchronous SDR Dual Port SRAM

Features

- True dual port memory enables simultaneous access to the shared array from each port
- Synchronous pipelined operation with Single Data Rate (SDR) operation on each port
  - SDR interface at 200 MHz
  - Up to 28.8 Gb/s bandwidth (200 MHz x 72 bit x 2 ports)
- Selectable pipelined or flow-through mode
- 1.5V or 1.8V core power supply
- Commercial and Industrial temperature
- IEEE 1149.1 JTAG boundary scan
- Available in 484-Ball PBGA (x72) and 256-Ball FBGA (x36 and x18) packages
- FullFlex72 family
  - 36 Mbit: 512K x 72 (CYD36S72V18)
  - 18 Mbit: 256K x 72 (CYD18S72V18)
  - 9 Mbit: 128K x 72 (CYD09S72V18)
  - 4 Mbit: 64K x 72 (CYD04S72V18)
- FullFlex36 family
  - 36 Mbit: 1M x 36 (CYD36S36V18)
  - 18 Mbit: 512K x 36 (CYD18S36V18)
  - 9 Mbit: 256K x 36 (CYD09S36V18)
  - 4 Mbit: 128K x 36 (CYD04S36V18)
  - 2 Mbit: 64K x 36 (CYD02S36V18)
- FullFlex18 family
  - 36 Mbit: 2M x 18 (CYD36S18V18)
  - 18 Mbit: 1M x 18 (CYD18S18V18)
  - 9 Mbit: 512K x 18 (CYD09S18V18)
  - 4 Mbit: 256K x 18 (CYD04S18V18)
- Built in deterministic access control to manage address collisions
  - Deterministic flag output upon collision detection
  - Collision detection on back-to-back clock cycles
  - First Busy Address readback
- Advanced features for improved high speed data transfer and flexibility
  - Variable Impedance Matching (VIM)
  - Echo clocks
  - Selectable LVTTL (3.3V), Extended HSTL (1.4V–1.9V), 1.8V LVCMOS, or 2.5V LVCMOS IO on each port
  - Burst counters for sequential memory access
  - Mailbox with interrupt flags for message passing
  - Dual Chip Enables for easy depth expansion

Functional Description

The FullFlex™ dual port SRAM families consist of 2 Mbit, 4 Mbit, 9 Mbit, 18 Mbit, and 36 Mbit synchronous, true dual port static RAMs that are high speed, low power 1.8V or 1.5V CMOS. Two ports are provided, enabling simultaneous access to the array. Simultaneous access to a location triggers deterministic access control. For FullFlex72 these ports operate independently with 72-bit bus widths and each port is independently configured for two pipelined stages. Each port is also configured to operate in pipelined or flow through mode.

The advanced features include the following:

- Built in deterministic access control to manage address collisions during simultaneous access to the same memory location
- Variable Impedance Matching (VIM) to improve data transmission by matching the output driver impedance to the line impedance
- Echo clocks to improve data transfer

To reduce the static power consumption, chip enables power down the internal circuitry. The number of latency cycles before a change in $\overline{CE0}$ or CE1 enables or disables the databus matches the number of cycles of read latency selected for the device. For a valid write or read to occur, activate both chip enable inputs on a port.

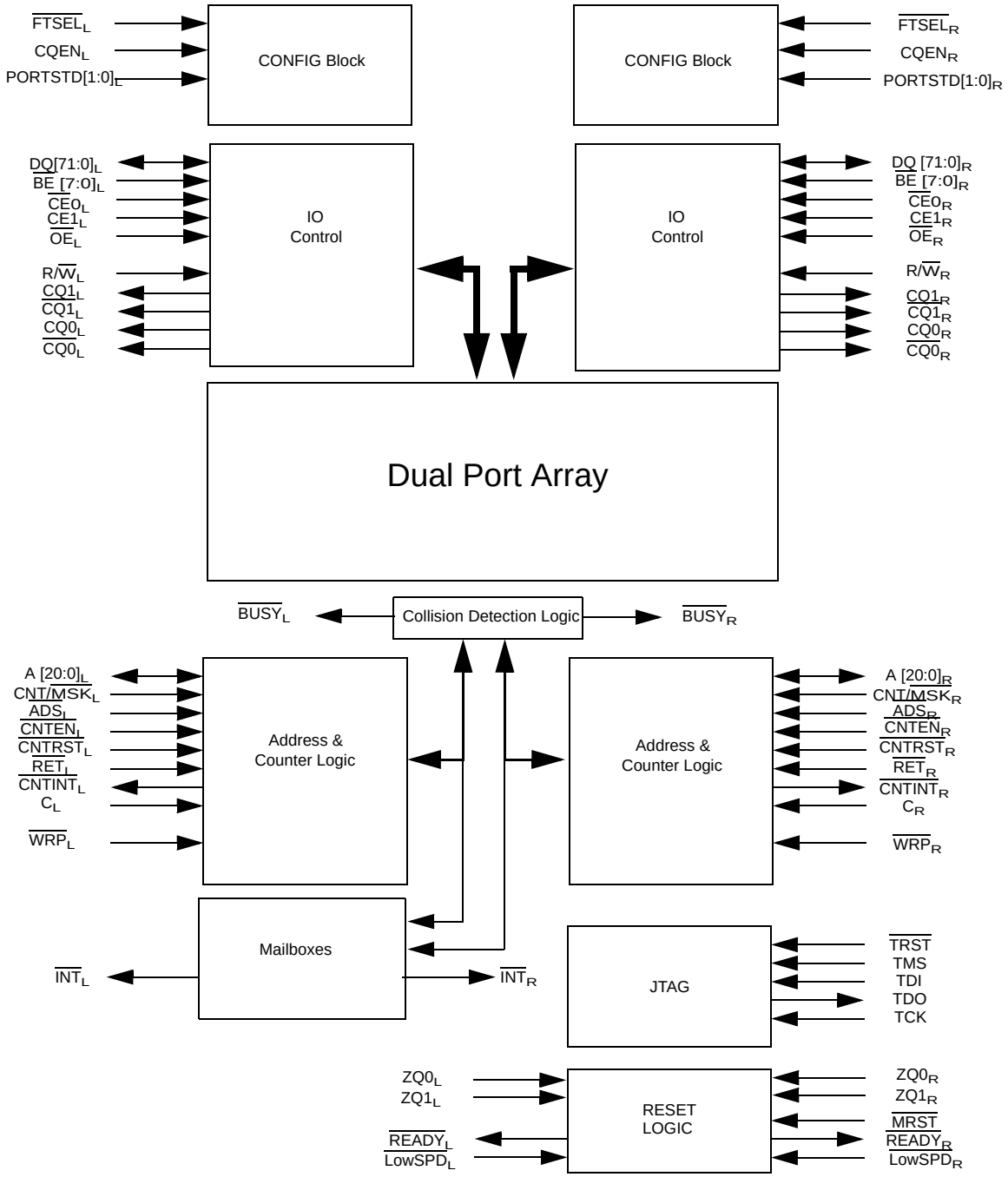
Each port contains an optional burst counter on the input address register. After externally loading the counter with the initial address, the counter increments the address internally.

Additional device features include a mask register and a mirror register to control counter increments and wrap around. The counter interrupt ($\overline{CNTINT}$) flags notify the host that the counter reaches maximum count value on the next clock cycle. The host reads the burst counter internal address, mask register address, and busy address on the address lines. The host also loads the counter with the address stored in the mirror register by using the retransmit functionality. Mailbox interrupt flags are used for message passing, and JTAG boundary scan and asynchronous Master Reset ($\overline{MRST}$) are also available. The Logic Block Diagram on page 2 shows these features.

The FullFlex72 is offered in a 484-Ball plastic BGA package. The FullFlex36 and FullFlex18 are available in 256-Ball fine pitch BGA package.

Logic Block Diagram

The Logic Block Diagram for FullFlex72, FullFlex36, and FullFlex18 family follows: [1, 2, 3]



Notes

1. The CYD36S18V18 device has 21 address bits. The CYD36S36V18 and CYD18S18V18 devices have 20 address bits. The CYD36S72V18, CYD18S36V18, and CYD09S18V18 devices have 19 address bits. The CYD18S72V18, CYD09S36V18, and CYD04S18V18 devices have 18 address bits. The CYD09S72V18 and CYD04S36V18 devices have 17 address bits. The CYD04S72V18 and CYD02S36V18 have 16 address bits.
2. The FullFlex72 family of devices has 72 data lines. The FullFlex36 family of devices has 36 data lines. The FullFlex18 family of devices has 18 data lines.
3. The FullFlex72 family of devices has eight byte enables. The FullFlex36 family of devices has four byte enables. The FullFlex18 family of devices has two byte enables.

Figure 1. FullFlex72 SDR 484-Ball BGA Pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	DNU	DQ61L	DQ59L	DQ57L	DQ54L	DQ51L	DQ48L	DQ45L	DQ42L	DQ39L	DQ36L	DQ36R	DQ39R	DQ42R	DQ45R	DQ48R	DQ51R	DQ54R	DQ57R	DQ59R	DQ61R	DNU
B	DQ63L	DQ62L	DQ60L	DQ58L	DQ55L	DQ52L	DQ49L	DQ46L	DQ43L	DQ40L	DQ37L	DQ37R	DQ40R	DQ43R	DQ46R	DQ49R	DQ52R	DQ55R	DQ58R	DQ60R	DQ62R	DQ63R
C	DQ65L	DQ64L	VSS	VSS	DQ56L	DQ53L	DQ50L	DQ47L	DQ44L	DQ41L	DQ38L	DQ38R	DQ41R	DQ44R	DQ47R	DQ50R	DQ53R	DQ56R	VSS	VSS	DQ64R	DQ65R
D	DQ67L	DQ66L	VSS	VSS	VSS	$\overline{CQ1L}$	CQ1L	VSS	$\overline{LOWS}$ PDL	PORTS TD0L	ZQ0L [4]	$\overline{BUSYL}$	$\overline{CNTIN}$ TL	PORTS TD1L	DNU	CQ1R	$\overline{CQ1R}$	VSS	VSS	VSS	DQ66R	DQ67R
E	DQ69L	DQ68L	VDDIO L	VSS	VSS	VDDIO L	VDDIO L	VDDIO L	VDDIO L	VDDIO L	VTTL	VTTL	VTTL	VDDIO R	VDDIO R	VDDIO R	VDDIO R	DNU	VSS	VDDIO R	DQ68R	DQ69R
F	DQ71L	DQ70L	CE1L	$\overline{CE0L}$	VDDIO L	VDDIO L	VDDIO L	VDDIO L	VDDIO L	VCORE	VCORE	VCORE	VCORE	VDDIO R	VDDIO R	VDDIO R	VDDIO R	VDDIO R	$\overline{CE0R}$	CE1R	DQ70R	DQ71R
G	A0L	A1L	$\overline{RETL}$	$\overline{BE4L}$	VDDIO L	VDDIO L	VREFL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VREFR	VDDIO R	VDDIO R	$\overline{BE4R}$	$\overline{RETR}$	A1R	A0R
H	A2L	A3L	$\overline{WRPL}$	$\overline{BE5L}$	VDDIO L	VDDIO L	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIO R	VDDIO R	$\overline{BE5R}$	$\overline{WRPR}$	A3R	A2R
J	A4L	A5L	$\overline{READY}$ L	$\overline{BE6L}$	VDDIO L	VDDIO L	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIO R	VDDIO R	$\overline{BE6R}$	$\overline{READY}$ R	A5R	A4R
K	A6L	A7L	ZQ1L [4, 5]	$\overline{BE7L}$	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VDDIO R	$\overline{BE7R}$	ZQ1R [4, 5]	A7R	A6R
L	A8L	A9L	CL	$\overline{OEL}$	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	$\overline{OER}$	CR	A9R	A8R
M	A10L	A11L	VSS	$\overline{BE3L}$	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	$\overline{BE3R}$	VSS	A11R	A10R
N	A12L	A13L	$\overline{ADSL}$	$\overline{BE2L}$	VDDIO L	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	$\overline{BE2R}$	$\overline{ADSR}$	A13R	A12R
P	A14L	A15L	CNT/$\overline{MSKL}$	$\overline{BE1L}$	VDDIO L	VDDIO L	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIO R	VDDIO R	$\overline{BE1R}$	CNT/$\overline{MSKR}$	A15R	A14R
R	A16L [8]	A17L [7]	$\overline{CNTENL}$	$\overline{BE0L}$	VDDIO L	VDDIO L	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIO R	VDDIO R	$\overline{BE0R}$	$\overline{CNTENR}$	A17R [7]	A16R [8]
T	A18L [6]	DNU	$\overline{CNTRSTL}$	$\overline{INTL}$	VDDIO L	VDDIO L	VREFL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VREFR	VDDIO R	VDDIO R	$\overline{INTR}$	$\overline{CNTRSTR}$	DNU	A18R [6]
U	DQ35L	DQ34L	R/$\overline{WL}$	CQENL	VDDIO L	VDDIO L	VDDIO L	VDDIO L	VDDIO L	VCORE	VCORE	VCORE	VCORE	VDDIO R	VDDIO R	VDDIO R	VDDIO R	VDDIO R	CQENR	R/$\overline{WR}$	DQ34R	DQ35R
V	DQ33L	DQ32L	$\overline{FTSELL}$	VDDIO L	DNU	VDDIO L	VDDIO L	VDDIO L	VDDIO L	VTTL	VTTL	VTTL	VDDIO R	VDDIO R	VDDIO R	VDDIO R	VDDIO R	$\overline{TRST}$	VDDIO R	$\overline{FTSELR}$	DQ32R	DQ33R
W	DQ31L	DQ30L	VSS	$\overline{MRST}$	VSS	$\overline{CQ0L}$	CQ0L	DNU	PORTS TD1R	$\overline{CNTINTR}$	$\overline{BUSYR}$	ZQ0R [4]	PORTS TD0R	$\overline{LOWS}$ PDR	VSS	CQ0R	$\overline{CQ0R}$	VSS	TDI	TDO	DQ30R	DQ31R
Y	DQ29L	DQ28L	VSS	VSS	DQ20L	DQ17L	DQ14L	DQ11L	DQ8L	DQ5L	DQ2L	DQ2R	DQ5R	DQ8R	DQ11R	DQ14R	DQ17R	DQ20R	TMS	TCK	DQ28R	DQ29R
AA	DQ27L	DQ26L	DQ24L	DQ22L	DQ19L	DQ16L	DQ13L	DQ10L	DQ7L	DQ4L	DQ1L	DQ1R	DQ4R	DQ7R	DQ10R	DQ13R	DQ16R	DQ19R	DQ22R	DQ24R	DQ26R	DQ27R
AB	DNU	DQ25L	DQ23L	DQ21L	DQ18L	DQ15L	DQ12L	DQ9L	DQ6L	DQ3L	DQ0L	DQ0R	DQ3R	DQ6R	DQ9R	DQ12R	DQ15R	DQ18R	DQ21R	DQ23R	DQ25R	DNU

Notes
4. Leave this ball unconnected to disable VIM.
5. This ball is applicable only for 36 Mbit and DNU for 18 Mbit and lower densities.
6. Leave this Ball unconnected for CYD18S72V18, CYD09S72V18, and CYD04S72V18.
7. Leave this Ball unconnected for CYD09S72V18 and CYD04S72V18.
8. Leave this Ball unconnected for CYD04S72V18.

Figure 2. FullFlex36 SDR 484-Ball BGA Pinout (Top View)[9]

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	DNU	DNU	DNU	DNU	DNU	DQ33L	DQ30L	DQ27L	DQ24L	DQ21L	DQ18L	DQ18R	DQ21R	DQ24R	DQ27R	DQ30R	DQ33R	DNU	DNU	DNU	DNU	DNU
B	DNU	DNU	DNU	DNU	DNU	DQ34L	DQ31L	DQ28L	DQ25L	DQ22L	DQ19L	DQ19R	DQ22R	DQ25R	DQ28R	DQ31R	DQ34R	DNU	DNU	DNU	DNU	DNU
C	DNU	DNU	VSS	VSS	DNU	DQ35L	DQ32L	DQ29L	DQ26L	DQ23L	DQ20L	DQ20R	DQ23R	DQ26R	DQ29R	DQ32R	DQ35R	DNU	VSS	VSS	DNU	DNU
D	DNU	DNU	VSS	VSS	VSS	$\overline{\text{CQ1L}}$	CQ1L	VSS	$\overline{\text{LOWS}}$ PDL	PORTSTD0L	ZQ0L [4]	$\overline{\text{BUSYL}}$	$\overline{\text{CNTIN}}$TL	PORTSTD1L	DNU	CQ1R	$\overline{\text{CQ1R}}$	VSS	VSS	VSS	DNU	DNU
E	DNU	DNU	VDDIOL	VSS	VSS	VDDIOL	VDDIOR	VDDIOR	VDDIOR	VDDIOR	VTTL	VTTL	VTTL	VDDIOL	VDDIOL	VDDIOL	VDDIOL	DNU	VSS	VDDIOR	DNU	DNU
F	DNU	DNU	CE1L	$\overline{\text{CE0L}}$	VDDIOL	VDDIOL	VDDIOR	VDDIOR	VDDIOR	VCORE	VCORE	VCORE	VCORE	VDDIOL	VDDIOL	VDDIOL	VDDIOR	VDDIOR	$\overline{\text{CE0R}}$	CE1R	DNU	DNU
G	A0L	A1L	$\overline{\text{RETL}}$	$\overline{\text{BE2L}}$	VDDIOL	VDDIOL	VREFL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VREFR	VDDIOR	VDDIOR	$\overline{\text{BE2R}}$	$\overline{\text{RETR}}$	A1R	A0R
H	A2L	A3L	$\overline{\text{WRPL}}$	$\overline{\text{BE3L}}$	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	$\overline{\text{BE3R}}$	$\overline{\text{WRPR}}$	A3R	A2R
J	A4L	A5L	$\overline{\text{READY}}$L	DNU	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	DNU	$\overline{\text{READY}}$R	A5R	A4R
K	A6L	A7L	ZQ1L [4]	DNU	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VDDIOR	DNU	ZQ1R [4]	A7R	A6R
L	A8L	A9L	CL	$\overline{\text{OEL}}$	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	$\overline{\text{OER}}$	CR	A9R	A8R
M	A10L	A11L	VSS	DNU	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	DNU	VSS	A11R	A10R
N	A12L	A13L	$\overline{\text{ADSL}}$	DNU	VDDIOL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	DNU	$\overline{\text{ADSR}}$	A13R	A12R
P	A14L	A15L	CNT/$\overline{\text{M}}$SKL	$\overline{\text{BE1L}}$	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	$\overline{\text{BE1R}}$	CNT/$\overline{\text{M}}$SKR	A15R	A14R
R	A16L	A17L	$\overline{\text{CNTEN}}$L	$\overline{\text{BE0L}}$	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	$\overline{\text{BE0R}}$	$\overline{\text{CNTEN}}$R	A17R	A16R
T	A18L	A19L	$\overline{\text{CNTRS}}$TL	$\overline{\text{INTL}}$	VDDIOL	VDDIOL	VREFL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VREFR	VDDIOR	VDDIOR	$\overline{\text{INTR}}$	$\overline{\text{CNTRS}}$TR	A19R	A18R
U	DNU	DNU	R/$\overline{\text{WL}}$	CQENL	VDDIOL	VDDIOL	VDDIOR	VDDIOR	VDDIOR	VCORE	VCORE	VCORE	VCORE	VDDIOL	VDDIOL	VDDIOL	VDDIOR	VDDIOR	CQENR	R/$\overline{\text{WR}}$	DNU	DNU
V	DNU	DNU	$\overline{\text{FTSEL}}$L	VDDIOL	DNU	VDDIOR	VDDIOR	VDDIOR	VDDIOR	VTTL	VTTL	VTTL	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VDDIOR	$\overline{\text{TRST}}$	VDDIOR	$\overline{\text{FTSEL}}$R	DNU	DNU
W	DNU	DNU	VSS	$\overline{\text{MRST}}$	VSS	$\overline{\text{CQ0L}}$	CQ0L	DNU	PORTSTD1R	$\overline{\text{CNTIN}}$TR	$\overline{\text{BUSYR}}$	ZQ0R [4]	PORTSTD0R	$\overline{\text{LOWS}}$PDR	VSS	CQ0R	$\overline{\text{CQ0R}}$	VSS	TDI	TDO	DNU	DNU
Y	DNU	DNU	VSS	VSS	DNU	DQ17L	DQ14L	DQ11L	DQ8L	DQ5L	DQ2L	DQ2R	DQ5R	DQ8R	DQ11R	DQ14R	DQ17R	DNU	TMS	TCK	DNU	DNU
AA	DNU	DNU	DNU	DNU	DNU	DQ16L	DQ13L	DQ10L	DQ7L	DQ4L	DQ1L	DQ1R	DQ4R	DQ7R	DQ10R	DQ13R	DQ16R	DNU	DNU	DNU	DNU	DNU
AB	DNU	DNU	DNU	DNU	DNU	DQ15L	DQ12L	DQ9L	DQ6L	DQ3L	DQ0L	DQ0R	DQ3R	DQ6R	DQ9R	DQ12R	DQ15R	DNU	DNU	DNU	DNU	DNU

Note
9. Use this pinout only for device CYD36S36V18 of the FullFlex36 family.

Figure 3. FullFlex18 SDR 484-Ball BGA Pinout (Top View)[10]

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DQ15L	DQ12L	DQ9L	DQ9R	DQ12R	DQ15R	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
B	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DQ16L	DQ13L	DQ10L	DQ10R	DQ13R	DQ16R	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
C	DNU	DNU	VSS	VSS	DNU	DNU	DNU	DNU	DQ17L	DQ14L	DQ11L	DQ11R	DQ14R	DQ17R	DNU	DNU	DNU	DNU	VSS	VSS	DNU	DNU
D	DNU	DNU	VSS	VSS	VSS	CQ1L	CQ1L	VSS	LOWSPDL	PORTSTD0L	ZQ0L[4]	BUSYL	CNTINTL	PORTSTD1L	DNU	CQ1R	CQ1R	VSS	VSS	VSS	DNU	DNU
E	DNU	DNU	VDDIOL	VSS	VSS	VDDIOL	VDDIOR	VDDIOR	VDDIOR	VDDIOR	VTTL	VTTL	VTTL	VDDIOL	VDDIOL	VDDIOL	VDDIOL	DNU	VSS	VDDIOR	DNU	DNU
F	DNU	DNU	CE1L	CE0L	VDDIOL	VDDIOL	VDDIOR	VDDIOR	VDDIOR	VCORE	VCORE	VCORE	VCORE	VDDIOL	VDDIOL	VDDIOL	VDDIOR	VDDIOR	CE0R	CE1R	DNU	DNU
G	A0L	A1L	RETL	BE1L	VDDIOL	VDDIOL	VREFL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VREFR	VDDIOR	VDDIOR	BE1R	RETR	A1R	A0R
H	A2L	A3L	WRPL	DNU	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	DNU	WRPR	A3R	A2R
J	A4L	A5L	READYL	DNU	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	DNU	READYR	A5R	A4R
K	A6L	A7L	ZQ1L[4]	DNU	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VDDIOR	DNU	ZQ1R[4]	A7R	A6R
L	A8L	A9L	CL	OEL	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	OER	CR	A9R	A8R
M	A10L	A11L	VSS	DNU	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	DNU	VSS	A11R	A10R
N	A12L	A13L	ADSL	DNU	VDDIOL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	DNU	ADSR	A13R	A12R
P	A14L	A15L	CNT/MSKL	DNU	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	DNU	CNT/MSKR	A15R	A14R
R	A16L	A17L	CNTENL	BE0L	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	BE0R	CNTENR	A17R	A16R
T	A18L	A19L	CNTRSTL	INTL	VDDIOL	VDDIOL	VREFL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VREFR	VDDIOR	VDDIOR	INTR	CNTRSTR	A19R	A18R
U	A20L	DNU	R/WL	CQENL	VDDIOL	VDDIOL	VDDIOR	VDDIOR	VDDIOR	VCORE	VCORE	VCORE	VCORE	VDDIOL	VDDIOL	VDDIOL	VDDIOR	VDDIOR	CQENR	R/WR	DNU	A20R
V	DNU	DNU	FTSELL	VDDIOL	DNU	VDDIOR	VDDIOR	VDDIOR	VDDIOR	VTTL	VTTL	VTTL	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VDDIOR	TRST	VDDIOR	FTSELR	DNU	DNU
W	DNU	DNU	VSS	MRST	VSS	CQ0L	CQ0L	DNU	PORTSTD1R	CNTINTR	BUSYR	ZQ0R[4]	PORTSTD0R	LOWSPDR	VSS	CQ0R	CQ0R	VSS	TDI	TDO	DNU	DNU
Y	DNU	DNU	VSS	VSS	DNU	DNU	DNU	DNU	DQ8L	DQ5L	DQ2L	DQ2R	DQ5R	DQ8R	DNU	DNU	DNU	DNU	TMS	TCK	DNU	DNU
AA	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DQ7L	DQ4L	DQ1L	DQ1R	DQ4R	DQ7R	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
AB	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DQ6L	DQ3L	DQ0L	DQ0R	DQ3R	DQ6R	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU

Note
10. Use this pinout only for device CYD36S18V18 of the FullFlex18 family.

Figure 4. FullFlex36 SDR 256-Ball BGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	DQ32L	DQ30L	DQ28L	DQ26L	DQ24L	DQ22L	DQ20L	DQ18L	DQ18R	DQ20R	DQ22R	DQ24R	DQ26R	DQ28R	DQ30R	DQ32R
B	DQ33L	DQ31L	DQ29L	DQ27L	DQ25L	DQ23L	DQ21L	DQ19L	DQ19R	DQ21R	DQ23R	DQ25R	DQ27R	DQ29R	DQ31R	DQ33R
C	DQ34L	DQ35L	$\overline{\text{RETL}}$	$\overline{\text{INTL}}$	CQ1L	$\overline{\text{CQ1L}}$	DNU	$\overline{\text{TRST}}$	$\overline{\text{MRST}}$	ZQ0R[4]	$\overline{\text{CQ1R}}$	CQ1R	$\overline{\text{INTR}}$	$\overline{\text{RETR}}$	DQ35R	DQ34R
D	A0L	A1L	$\overline{\text{WRPL}}$	VREFL	$\overline{\text{FTSELL}}$	$\overline{\text{LOWSPDL}}$	VSS	VTTL	VTTL	VSS	$\overline{\text{LOWSPDR}}$	$\overline{\text{FTSELR}}$	VREFR	$\overline{\text{WRPR}}$	A1R	A0R
E	A2L	A3L	$\overline{\text{CE0L}}$	CE1L	VDDIOL	VDDIOL	VDDIOL	VCORE	VCORE	VDDIOR	VDDIOR	VDDIOR	CE1R	$\overline{\text{CE0R}}$	A3R	A2R
F	A4L	A5L	$\overline{\text{CNTINTL}}$	$\overline{\text{BE3L}}$	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	$\overline{\text{BE3R}}$	$\overline{\text{CNTINTR}}$	A5R	A4R
G	A6L	A7L	$\overline{\text{BUSYL}}$	$\overline{\text{BE2L}}$	ZQ0L[4]	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	$\overline{\text{BE2R}}$	$\overline{\text{BUSYR}}$	A7R	A6R
H	A8L	A9L	CL	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	CR	A9R	A8R
J	A10L	A11L	VSS	PORTSTD1L	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	PORTSTD1R	VSS	A11R	A10R
K	A12L	A13L	$\overline{\text{OEL}}$	$\overline{\text{BE1L}}$	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	$\overline{\text{BE1R}}$	$\overline{\text{OER}}$	A13R	A12R
L	A14L	A15L	$\overline{\text{ADSL}}$	$\overline{\text{BE0L}}$	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	$\overline{\text{BE0R}}$	$\overline{\text{ADSR}}$	A15R	A14R
M	A16L[13]	A17L[12]	R/$\overline{\text{WL}}$	CQENL	VDDIOL	VDDIOL	VDDIOL	VCORE	VCORE	VDDIOR	VDDIOR	VDDIOR	CQENR	R/$\overline{\text{WR}}$	A17R[12]	A16R[13]
N	A18L[11]	DNU	CNT/$\overline{\text{MSK}}$L	VREFL	PORTSTD0L	$\overline{\text{READYL}}$	DNU	VTTL	VTTL	DNU	$\overline{\text{READYR}}$	PORTSTD0R	VREFR	CNT/$\overline{\text{MSK}}$R	DNU	A18R[11]
P	DQ16L	DQ17L	$\overline{\text{CNTENL}}$	$\overline{\text{CNTRSTL}}$	CQ0L	$\overline{\text{CQ0L}}$	TCK	TMS	TDO	TDI	$\overline{\text{CQ0R}}$	CQ0R	$\overline{\text{CNTRSTR}}$	$\overline{\text{CNTENR}}$	DQ17R	DQ16R
R	DQ15L	DQ13L	DQ11L	DQ9L	DQ7L	DQ5L	DQ3L	DQ1L	DQ1R	DQ3R	DQ5R	DQ7R	DQ9R	DQ11R	DQ13R	DQ15R
T	DQ14L	DQ12L	DQ10L	DQ8L	DQ6L	DQ4L	DQ2L	DQ0L	DQ0R	DQ2R	DQ4R	DQ6R	DQ8R	DQ10R	DQ12R	DQ14R

Notes
11. Leave this ball unconnected for CYD09S36V18, CYD04S36V18, and CYD02S36V18.
12. Leave this ball unconnected for CYD04S36V18 and CYD02S36V18.
13. Leave this ball unconnected for CYD02S36V18.

Figure 5. FullFlex18 SDR 256-Ball BGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	DNU	DNU	DNU	DQ17L	DQ16L	DQ13L	DQ12L	DQ9L	DQ9R	DQ12R	DQ13R	DQ16R	DQ17R	DNU	DNU	DNU
B	DNU	DNU	DNU	DNU	DQ15L	DQ14L	DQ11L	DQ10L	DQ10R	DQ11R	DQ14R	DQ15R	DNU	DNU	DNU	DNU
C	DNU	DNU	$\overline{\text{RETL}}$	$\overline{\text{INTL}}$	CQ1L	$\overline{\text{CQ1L}}$	DNU	$\overline{\text{TRST}}$	$\overline{\text{MRST}}$	ZQ0R[4]	$\overline{\text{CQ1R}}$	CQ1R	$\overline{\text{INTR}}$	$\overline{\text{RETR}}$	DNU	DNU
D	A0L	A1L	$\overline{\text{WRPL}}$	VREFL	$\overline{\text{FTSELL}}$	$\overline{\text{LOWSPDL}}$	VSS	VTTL	VTTL	VSS	$\overline{\text{LOWSPDR}}$	$\overline{\text{FTSELR}}$	VREFR	$\overline{\text{WRPR}}$	A1R	A0R
E	A2L	A3L	$\overline{\text{CE0L}}$	CE1L	VDDIOL	VDDIOL	VDDIOL	VCORE	VCORE	VDDIOR	VDDIOR	VDDIOR	CE1R	$\overline{\text{CE0R}}$	A3R	A2R
F	A4L	A5L	$\overline{\text{CNTINTL}}$	DNU	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	DNU	$\overline{\text{CNTINTR}}$	A5R	A4R
G	A6L	A7L	$\overline{\text{BUSYL}}$	DNU	ZQ0L[4]	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	DNU	$\overline{\text{BUSYR}}$	A7R	A6R
H	A8L	A9L	CL	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	CR	A9R	A8R
J	A10L	A11L	VSS	PORTSTD1L	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	PORTSTD1R	VSS	A11R	A10R
K	A12L	A13L	$\overline{\text{OEL}}$	$\overline{\text{BE1L}}$	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	$\overline{\text{BE1R}}$	$\overline{\text{OER}}$	A13R	A12R
L	A14L	A15L	$\overline{\text{ADSL}}$	$\overline{\text{BE0L}}$	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	$\overline{\text{BE0R}}$	$\overline{\text{ADSR}}$	A15R	A14R
M	A16L	A17L	R/$\overline{\text{WL}}$	CQENL	VDDIOL	VDDIOL	VDDIOL	VCORE	VCORE	VDDIOR	VDDIOR	VDDIOR	CQENR	R/$\overline{\text{WR}}$	A17R	A16R
N	A18L[15]	A19L[14]	CNT/$\overline{\text{MSK}}$L	VREFL	PORTSTD0L	$\overline{\text{READYL}}$	DNU	VTTL	VTTL	DNU	$\overline{\text{READYR}}$	PORTSTD0R	VREFR	CNT/$\overline{\text{MSK}}$R	A19R[14]	A18R[15]
P	DNU	DNU	$\overline{\text{CNTENL}}$	$\overline{\text{CNTRSTL}}$	CQ0L	$\overline{\text{CQ0L}}$	TCK	TMS	TDO	TDI	$\overline{\text{CQ0R}}$	CQ0R	$\overline{\text{CNTRSTR}}$	$\overline{\text{CNTENR}}$	DNU	DNU
R	DNU	DNU	DNU	DNU	DQ6L	DQ5L	DQ2L	DQ1L	DQ1R	DQ2R	DQ5R	DQ6R	DNU	DNU	DNU	DNU
T	DNU	DNU	DNU	DQ8L	DQ7L	DQ4L	DQ3L	DQ0L	DQ0R	DQ3R	DQ4R	DQ7R	DQ8R	DNU	DNU	DNU

Notes
14. Leave this ball unconnected for CYD09S18V18 and CYD04S18V18.
15. Leave this ball unconnected for CYD04S18V18.

Selection Guide

Parameter	–200	–167	Unit
f_{MAX}[17]	200	167	MHz
Maximum Access Time (Clock to Data)	3.3	4.0	ns
Typical Operating Current I_{CC}	800[16]	700[16]	mA
Typical Standby Current for I_{SB3} (Both Ports CMOS Level)	210[16]	210[16]	mA

Pin Definitions

Left Port	Right Port	Description
$A[20:0]_L$	$A[20:0]_R$	**Address Inputs**.[1]
$DQ[71:0]_L$	$DQ[71:0]_R$	**Data Bus Input and Output**.[2]
$\overline{BE}[7:0]_L$	$\overline{BE}[7:0]_R$	**Byte Select Inputs**.[3] Asserting these signals enables read and write operations to the corresponding bytes of the memory array.
$\overline{BUSY}_L$	$\overline{BUSY}_R$	**Port Busy Output**. When there is an address match and both chip enables are active for both ports, an external BUSY signal is asserted on the fifth clock cycles from when the collision occurs.
C_L	C_R	**Clock Signal**. Maximum clock input rate is f_{MAX}.
$\overline{CE0}_L$	$\overline{CE0}_R$	**Active LOW Chip Enable Input**.
$CE1_L$	$CE1_R$	**Active HIGH Chip Enable Input**.
$CQEN_L$	$CQEN_R$	**Echo Clock Enable Input**. Assert HIGH to enable echo clocking on respective port.
$CQ0_L$	$CQ0_R$	**Echo Clock Signal Output for DQ[35:0] for FullFlex72 Devices**. Echo Clock Signal Output for DQ[17:0] for FullFlex36 devices. Echo Clock Signal Output for DQ[8:0] for FullFlex18 devices.
$\overline{CQ0}_L$	$\overline{CQ0}_R$	**Inverted Echo Clock Signal Output for DQ[35:0] for FullFlex72 Devices**. Inverted Echo Clock Signal Output for DQ[17:0] for FullFlex36 devices. Inverted Echo Clock Signal Output for DQ[8:0] for FullFlex18 devices.
$CQ1_L$	$CQ1_R$	**Echo Clock Signal Output for DQ[71:36] for FullFlex72 Devices**. Echo Clock Signal Output for DQ[35:18] for FullFlex36 devices. Echo Clock Signal Output for DQ[17:9] for FullFlex18 devices.
$\overline{CQ1}_L$	$\overline{CQ1}_R$	**Inverted Echo Clock Signal Output for DQ[71:36] for FullFlex72 Devices**. Inverted Echo Clock Signal Output for DQ[35:18] for FullFlex36 devices. Inverted Echo Clock Signal Output for DQ[17:9] forFullFlex18 devices.
$ZQ[1:0]_L$	$ZQ[1:0]_R$	**VIM Output Impedance Matching Input**.[18] To use, connect a calibrating resistor between ZQ and ground. The resistor must be five times larger than the intended line impedance driven by the dual port. Assert HIGH or leave DNU to disable VIM.
$\overline{OE}_L$	$\overline{OE}_R$	**Output Enable Input**. This asynchronous signal must be asserted LOW to enable the DQ data pins during read operations.
$\overline{INT}_L$	$\overline{INT}_R$	**Mailbox Interrupt Flag Output**. The mailbox permits communications between ports. The upper two memory locations are used for message passing. $\overline{INT}_L$ is asserted LOW when the right port writes to the mailbox location of the left port, and vice versa. An interrupt to a port is deasserted HIGH when it reads the contents of its mailbox.
$\overline{LowSPD}_L$	$\overline{LowSPD}_R$	**Port Low Speed Select Input**. Assert this pin LOW to disable the DLL. For operation at less than 100 MHz, assert this pin LOW.

Notes
16. For 18 Mbit x72 commercial configuration only, refer to Electrical Characteristics on page 18 for complete information.
17. SDR mode with two pipelined stages.
18. The pin ZQ[1] is applicable only for 36 Mbit devices. This pin is DNU for 18 Mbit and lower density devices.

Pin Definitions (continued)

Left Port	Right Port	Description
$PORTSTD[1:0]_L$[19]	$PORTSTD[1:0]_R$[19]	**Port Clock/Address/Control/Data/Echo Clock/I/O Standard Select Input**. Assert these pins LOW/LOW for LVTTL, LOW/HIGH for HSTL, HIGH/LOW for 2.5V LVCMOS, and HIGH/HIGH for 1.8V LVCMOS, respectively. These pins are driven by VTTL referenced levels.
$R/\overline{W}_L$	$R/\overline{W}_R$	**Read/Write Enable Input**. Assert this pin LOW to write to, or HIGH to read from the dual port memory array.
$\overline{READY}_L$	$\overline{READY}_R$	**Port DLL Ready Output**. This signal is asserted LOW when the DLL and Variable Impedance Matching circuits complete calibration. This is a wired OR capable output.
$CNT/\overline{MSK}_L$	$CNT/\overline{MSK}_R$	**Port Counter/$\overline{\text{Mask}}$ Select Input**. Counter control input.
$\overline{ADS}_L$	$\overline{ADS}_R$	**Port Counter Address Load Strobe Input**. Counter control input.
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	**Port Counter Enable Input**. Counter control input.
$\overline{CNTRST}_L$	$\overline{CNTRST}_R$	**Port Counter Reset Input**. Counter control input.
$\overline{CNTINT}_L$	$\overline{CNTINT}_R$	**Port Counter Interrupt Output**. This pin is asserted LOW one cycle before the unmasked portion of the counter is incremented to all “1s”.
$\overline{WRP}_L$	$\overline{WRP}_R$	**Port Counter Wrap Input**. When the burst counter reaches the maximum count, on the next counter increment $\overline{WRP}$ is set LOW to load the unmasked counter bits to 0. It is set HIGH to load the counter with the value stored in the mirror register.
$\overline{RET}_L$	$\overline{RET}_R$	**Port Counter Retransmit Input**. Assert this pin LOW to reload the initial address for repeated access to the same segment of memory.
$VREF_L$	$VREF_R$	**Port External HSTL IO Reference Input**. This pin is left DNU when HSTL is not used.
$VDDIO_L$	$VDDIO_R$	**Port Data IO Power Supply**.
$\overline{FTSEL}_L$	$\overline{FTSEL}_R$	**Port Flow through Mode Select Input**. Assert this pin LOW to select Flow through mode. Assert this pin HIGH to select Pipelined mode.
$\overline{MRST}$		**Master Reset Input**. $\overline{MRST}$ is an asynchronous input signal and affects both ports. Asserting $\overline{MRST}$ LOW performs all of the reset functions as described in the text. A $\overline{MRST}$ operation is required at power up. This pin is driven by a $VDDIO_L$ referenced signal.
TMS		**JTAG Test Mode Select Input**. It controls the advance of JTAG TAP state machine. State machine transitions occur on the rising edge of TCK. Operation for LVTTL or 2.5V LVCMOS.
TDI		**JTAG Test Data Input**. Data on the TDI input is shifted serially into selected registers. Operation for LVTTL or 2.5V LVCMOS.
$\overline{TRST}$		**JTAG Reset Input**. Operation for LVTTL or 2.5V LVCMOS.
TCK		**JTAG Test Clock Input**. Operation for LVTTL or 2.5V LVCMOS.
TDO		**JTAG Test Data Output**. TDO transitions occur on the falling edge of TCK. TDO is normally tri-stated except when captured data is shifted out of the JTAG TAP. Operation for LVTTL or 2.5V LVCMOS.
VSS		**Ground Inputs**.
VCORE		**Device Core Power Supply**.
VTTL		**LVTTL Power Supply**.

Note
19. $PORTSTD[1:0]_L$ and $PORTSTD[1:0]_R$ have internal pull down resistors.

Selectable IO Standard

The FullFlex device families offer the option to choose one of the four port standards for the device. Each port independently selects standards from single ended HSTL class I, single ended LVTTL, 2.5V LVCMOS, or 1.8V LVCMOS. The selection of the standard is determined by the PORTSTD pins for each port. These pins must be connected to an LVTTL power suppy. This determines the input clock, address, control, data, and Echo clock standard for each port as shown in Table 1.

Table 1. Port Standard Selection

PORTSTD1	PORTSTD0	I/O Standard
VSS	VSS	LVTTL
VSS	VTTL	HSTL
VTTL	VSS	2.5V LVCMOS
VTTL	VTTL	1.8V LVCMOS

Clocking

Separate clocks synchronize the operations on each port. Each port has one clock input C. In this mode, all the transactions on the address, control, and data are on the C rising edge. All transactions on the address, control, data input, output, and byte enables occur on the C rising edge.

Table 2. Data Pin Assignment

$\overline{BE}$ Pin Name	Data Pin Name
$\overline{BE}$[7]	DQ[71:63]
$\overline{BE}$[6]	DQ[62:54]
$\overline{BE}$[5]	DQ[53:45]
$\overline{BE}$[4]	DQ[44:36]
$\overline{BE}$[3]	DQ[35:27]
$\overline{BE}$[2]	DQ[26:18]
$\overline{BE}$[1]	DQ[17:9]
$\overline{BE}$[0]	DQ[8:0]

Selectable Pipelined or Flow through Mode

To meet data rate and throughput requirements, the FullFlex families offer selectable pipelined or flow through mode. Echo clocks are not supported in flow through mode and the DLL must be disabled.

Flow through mode is selected by the $\overline{FTSEL}$ pin. Strapping this pin HIGH selects pipelined mode. Strapping this pin LOW selects flow through mode.

DLL

The FullFlex familes of devices have an on-chip DLL. Enabling the DLL reduces the clock to data valid (t_{CD}) time enabling more setup time for the receiving device. For operation below 100 MHz, the DLL must be disabled. This is selectable by strapping LowSPD low.

Whenever the operating frequency is altered beyond the Clock Input Cycle to Cycle Jitter specification, reset the DLL, followed by 1024 clocks before any valid operation.

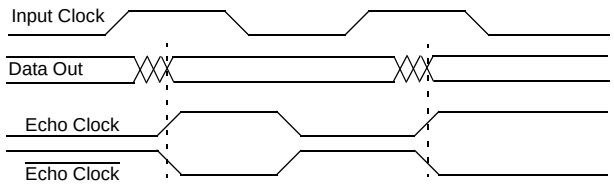
$\overline{LowSPD}$ pins are used to reset the DLLs for a single port independent of all other circuitry. MRST is used to reset all DLLs on the chip. For more information on DLL lock and reset time, see Master Reset on page 17.

Echo Clocking

As the speed of data increases, on-board delays caused by parasitics make it extremely difficult to provide accurate clock trees. To counter this problem, the FullFlex families incorporate Echo Clocks. Echo Clocks are enabled on a per port basis. The dual port receives input clocks that are used to clock in the address and control signals for a read operation. The dual port retransmits the input clocks relative to the data output. The buffered clocks are provided on the CQ1/$\overline{CQ1}$ and CQ0/$\overline{CQ0}$ outputs. Each port has a pair of Echo clocks. Each clock is associated with half the data bits. The output clock matches the corresponding ports IO configuration.

To enable echo clock outputs, tie CQEN HIGH. To disable echo clock outputs, tie CQEN LOW.

Figure 6. SDR Echo Clock Delay



Deterministic Access Control

Deterministic Access Control is provided for ease of design. The circuitry detects when both ports access the same location and provides an external $\overline{BUSY}$ flag to the port on which data is corrupted. The collision detection logic saves the address in conflict (Busy Address) to a readable register. In the case of multiple collisions, the first busy address is written to the busy address register.

If both ports access the same location at the same time and only one port is doing a write, if t_{CCS} is met, then the data written to and read from the address is valid data. For example, if the right port is reading and the left port is writing and the left ports clock meets t_{CCS}, then the data read from the address by the right port is the old data. In the same case, if the right ports clock meets t_{CCS}, then the data read out of the address from the right port is the new data. In the above case, if t_{CCS} is violated by the either ports clock with respect to the other port and the right port gets the external $\overline{BUSY}$ flag, the data from the right port is corrupted. Table 3 on page 11 shows the t_{CCS} timing that must be met to guarantee the data.

Table 4 on page 11 shows that, in the case of the left port writing and the right port reading, when an external $\overline{BUSY}$ flag is asserted on the right port, the data read out of the device is not guaranteed.

The value in the busy address register is read back to the address lines. The required input control signals for this function are shown in Table 7 on page 13. The value in the busy address register is read out to the address lines t_{CA} after the same amount of latency as a data read operation. After an initial address match, the $\overline{BUSY}$ flag is asserted and the address under contention is saved in the busy address register. All the following

address matches enable to generate the $\overline{BUSY}$ flag. However, none of the addresses are saved into the busy address register. When a busy readback is performed, the address of the first match that happens at least two clocks cycles after the busy readback is saved into the busy address register.

Table 3. t_{CCS} Timing for All Operating Modes

Port A—Early Arriving Port		Port B—Late Arriving Port		t_{CCS} C Rise to Opposite C Rise Setup Time for Non Corrupt Data	Unit
Mode	Active Edge	Mode	Active Edge		
SDR	C	SDR	C	$t_{CYC(min)} - 0.5$	ns

Table 4. Deterministic Access Control Logic

Left Port	Right Port	Left Clock	Right Clock	$\overline{BUSY}_L$	$\overline{BUSY}_R$	Description
Read	Read	X	X	H	H	No Collision
Write	Read	$>t_{CCS}$	0	H	H	Read OLD Data
		0	$>t_{CCS}$	H	H	Read NEW Data
		$<t_{CCS}$	0	H	H	Read OLD Data
				H	L	Data Not Guaranteed
		0	$<t_{CCS}$	H	H	Read NEW Data
				H	L	Data Not Guaranteed
Read	Write	$>t_{CCS}$	0	H	H	Read NEW Data
		0	$>t_{CCS}$	H	H	Read OLD Data
		$<t_{CCS}$	0	H	H	Read NEW Data
				L	H	Data Not Guaranteed
		0	$<t_{CCS}$	H	H	Read OLD Data
				L	H	Data Not Guaranteed
Write	Write	0	$>-t_{CCS}$ & $<t_{CCS}$	L	L	Array Data Corrupted
		0	$>t_{CCS}$	L	H	Array Stores Right Port Data
		$>t_{CCS}$	0	H	L	Array Stores Left Port Data

Variable Impedance Matching

Each port contains a Variable Impedance Matching circuit to set the impedance of the IO driver to match the impedance of the on-board traces. The impedance is set for all outputs except JTAG and is done by port. To take advantage of the VIM feature, connect a calibrating resistor (RQ) that is five times the value of the intended line impedance from the $ZQ_{[1:0]}$[18] pin to VSS. The output impedance is then adjusted to account for drifts in supply voltage and temperature every 1024 clock cycles. If a port's clock is suspended, the VIM circuit retains its last setting until the clock is restarted. On restart, it then resumes periodic adjustment. In the case of a significant change in device temperature or supply voltage, recalibration happens every 1024 clock cycles. A Master Reset initializes the VIM circuitry. Table 5 shows the VIM parameters and Table 6 describes the VIM operation modes.

To disable VIM, connect the ZQ pin to VDDIO of the relative supply for the IOs before a Master Reset.

Table 5. Variable Impedance Matching Parameters

Parameter	Min	Max	Unit	Tolerance
RQ Value	100	275	Ω	± 2%
Output Impedance	20	55	Ω	± 15%
Reset Time	N/A	1024	Cycles	N/A
Update Time	N/A	1024	Cycles	N/A

Table 6. Variable Impedance Matching Operation

RQ Connection	Output Configuration
100Ω - 275Ω to VSS	Output Driver Impedance = RQ/5 ± 15% at Vout = VDDIO/2
ZQ to VDDIO	VIM Disabled. Rout ≤ 20Ω at Vout = VDDIO/2

Address Counter and Mask Register Operations [1]

Each port of the FullFlex family contains a programmable burst address counter. The burst counter contains four registers: a counter register, a mask register, a mirror register, and a busy address register.

The **counter register** contains the address used to access the RAM array. It is changed only by the Master Reset (MRST), Counter Reset, Counter Load, Retransmit, and Counter Increment operations.

The **mask register** value affects the Counter Increment and Counter Reset operations by preventing the corresponding bits of the counter register from changing. It also affects the counter interrupt output (CNTINT). The mask register is only changed by Mask Reset, Mask Load, and MRST. The Mask Load operation loads the value of the address bus into the mask register. The mask register defines the counting range of the counter register. The mask register is divided into two or three consecutive regions. Zero or more 0s define the masked region and one or more 1s define the unmasked portion of the counter register. The counter register may be divided up to three regions. The region containing the least significant bits must be no more than two 0s. Bits one and zero may be 10 respectively, masking the least significant counter bit and causing the counter to increment by two instead of one. If bits one and zero are 00, the two least significant bits are masked and the counter increments by four instead of one. For example, in the case of a 256Kx72 configuration, a mask register value of 003FC divides the mask register into three regions. With bit 0 being the least significant bit and bit 17 being the most significant bit, the two least significant bits are masked, the next eight bits are unmasked, and the remaining bits are masked.

The **mirror register** reloads a counter register on retransmit operations (see Retransmit on page 14) and wrap functions (see Counter Interrupt on page 14 below). The last value loaded into the counter register is stored in the mirror register. The mirror register is only changed by master reset (MRST), counter reset, and counter load.

Table 7 on page 13 summarizes the operations of these registers and the required input control signals. All signals except MRST are synchronized to the ports clock.

Counter Load Operation [1]

The address counter and mirror registers are loaded with the address value presented on the address lines. This value ranges from 0 to 1FFFFF.

Mask Load Operation [1]

The mask register is loaded with the address value presented on the address bus. This value ranges from 0 to 1FFFFF though not all values permit correct increment operations. Permitted values are in the form of 2^n–1, 2^n–2, or 2^n–4. The counter register is only segmented up to three regions. From the most significant bit to the least significant bit, permitted values have zero or more 0s, one or more 1s, and the least significant two bits are 11, 10, or 00. Thus 1FFFFE, 07FFFF, and 003FFC are permitted values but 02FFFF, 003FFA, and 07FFE4 are not.

Counter Readback Operation

The internal value of the counter register is read out on the address lines. The address is valid t_{CA} after the selected number of latency cycles configured by FTSEL. The data bus (DQ) is tri-stated on the cycle that the address is presented on the address lines. Figure 7 on page 15 shows a block diagram of this logic.

Mask Readback Operation

The internal value of the mask register is read out on the address lines. The address is valid t_{CA} after the selected number of latency cycles configured by FTSEL. The data bus (DQ) is tri-stated on the cycle that the address is presented on the address lines. Figure 7 on page 15 shows a block diagram of the operation.

Counter Reset Operation

All unmasked bits of the counter and mirror registers are reset to ‘0’. All masked bits remain unchanged. A mask reset followed by a counter reset resets the counter and mirror registers to 00000.

Mask Reset Operation

The mask register is reset to all 1s, that unmasks every bit of the burst counter.

Table 7. Burst Counter and Mask Register Control Operations

The burst counter and mask register control operation for any port follows. [20, 21]

C	$\overline{MRST}$	$\overline{CNTRST}$	CNT/$\overline{MSK}$	$\overline{CNTEN}$	$\overline{ADS}$	$\overline{RET}$	Operation	Description
X	L	X	X	X	X	X	Master Reset	Reset address counter to all 0s, mask register to all 1s, and busy address to all 0s.
⎍	H	L	H	X	X	X	Counter Reset	Reset counter and mirror unmasked portion to all 0s.
⎍	H	L	L	X	X	X	Mask Reset	Reset mask register to all 1s.
⎍	H	H	H	L	L	X	Counter Load	Load burst counter and mirror with external address value presented on address lines.
⎍	H	H	L	L	L	X	Mask Load	Load mask register with value presented on the address lines.
⎍	H	H	H	L	H	L	Retransmit	Load counter with value in the mirror register.
⎍	H	H	H	L	H	H	Counter Increment	Internally increment address counter value.
⎍	H	H	H	H	H	H	Counter Hold	Constantly hold the address value for multiple clock cycles.
⎍	H	H	H	H	L	H	Counter Readback	Read out counter internal value on address lines.
⎍	H	H	L	H	L	H	Mask Readback	Read out mask register value on address lines.
⎍	H	H	L	H	H	L	Busy Address Readback	Read out first busy address after last busy address readback.
⎍	H	H	L	L	H	X	Reserved	
⎍	H	H	L	H	L	L	Reserved	
⎍	H	H	L	H	H	H	Reserved	
⎍	H	H	H	H	L	L	Reserved	
⎍	H	H	H	H	H	L	Reserved	

Notes
20. “X” = Don’t Care, “H” = HIGH, “L” = LOW.
21. Counter operation and mask register operation is independent of chip enables.

Increment Operation[1]

After the address counter is initially loaded with an external address, the counter can internally increment the address value and address the entire memory array. Only the unmasked bits of the counter register are incremented. For a counter bit to change, the corresponding bit in the mask register must be 1. If the two least significant bits of the mask register are 11, the burst counter increments by one. If the two least significant bits are 10, the burst counter increments by two, and if they are 00, the burst counter increments by four. If all unmasked counter bits are incremented to 1 and WRP is deasserted, the next increment l wraps the counter back to the initially loaded value. The cycle before the increment that results in all unmasked counter bits to become 1s, a counter interrupt flag (CNTINT) is asserted if the counter is incremented again. This increment causes the counter to reach its maximum value and the next increment returns the counter register to its initial value that was stored in the mirror register if WRP is deasserted. If WRP is asserted, the unmasked portion of the counter is filled with 0 instead. The example shown in Figure 8 on page 16 shows an example of the CYDD36S18V18 device with the mask register loaded with a mask value of 00007F unmasking the seven least significant bits. Setting the mask register to this value enables the counter to access the entire memory space. The address counter is then loaded with an initial value of 000005 assuming WRP is deasserted. The masked bits, the seventh address through the twenty-first address, do not increment in an increment operation. The counter address starts at address 000005 and increments its internal address value until it reaches the mask register value of 00007F. The counter wraps around the memory block to location 000005 at the next count. CNTINT is issued when the counter reaches the maximum –1 count.

Hold Operation

The value of all three registers is constantly maintained unchanged for an unlimited number of clock cycles. This operation is useful in applications where wait states are needed or when address is available a few cycles ahead of data in a shared bus interface.

Retransmit

Retransmit enables repeated access to the same block of memory without the need to reload the initial address. An internal mirror register stores the address counter value last loaded. While RET is asserted low, the counter continues to wrap back to the value in the mirror register independent of the state of WRP.

Counter Interrupt

The counter interrupt (CNTINT) is asserted LOW one clock cycle before an increment operation that results in the unmasked portion of the counter register being all 1s. It is deasserted by counter reset, counter load, mask reset, mask load, and MRST.

Counting by Two

When the two least significant bits of the mask register are 10, the counter increments by two.

Counting by Four

When the two least significant bits of the mask register are 00, the counter increments by four.

Mailbox Interrupts

Use the upper two memory locations for message passing and permit communications between ports. Table 8 on page 16 shows the interrupt operation for both ports. The highest memory location is the mailbox for the right port and the maximum address – 1 is the mailbox for the left port.

When one port writes to the other port's mailbox, the INT flag of the port that the mailbox belongs to is asserted LOW. The INT flag remains asserted until the mailbox location is read by the other port. When a port reads its mailbox, the INT flag is deasserted high after one cycle of latency with respect to the input clock of the port to which the mailbox belongs and is independent of OE.

As shown in Table 8 on page 16, to set the $\overline{INT}_R$ flag, a write operation by the left port to address 1FFFFF asserts $\overline{INT}_R$ LOW. A valid read of the 1FFFFF location by the right port resets $\overline{INT}_R$ HIGH after one cycle of latency with respect to the right port's clock. You must activate at least one byte enable to set or reset the mailbox interrupt.

Figure 7. Counter, Mask, and Mirror Logic Block Diagram

Figure 7 shows the counter, mask, and mirror logic block diagram. [1]

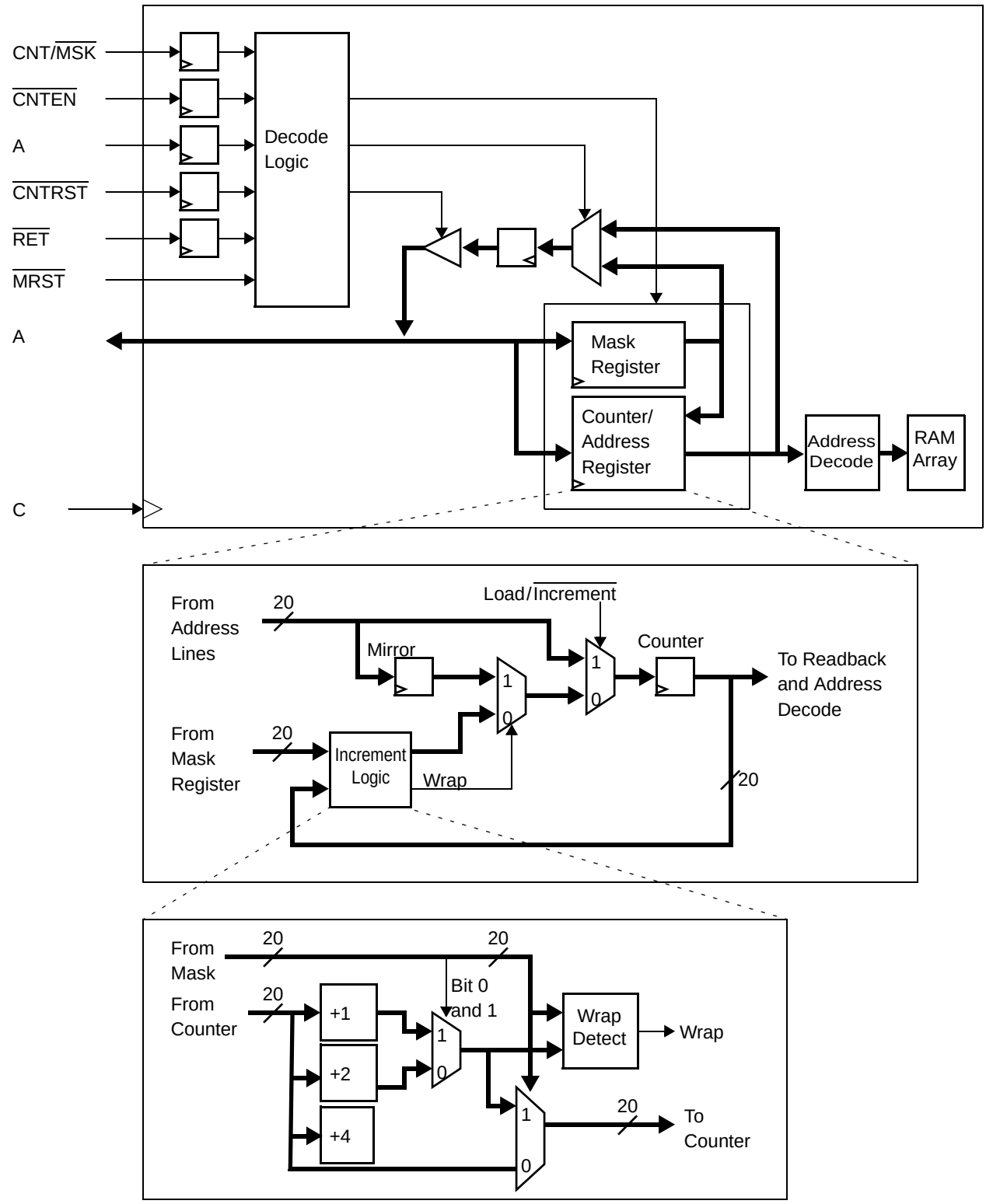


Figure 8. Programmable Counter-Mask Register Operation with $\overline{WRP}$ deasserted

Figure 8 shows the programmable counter-mask operation with WRP deasserted. [1, 25]

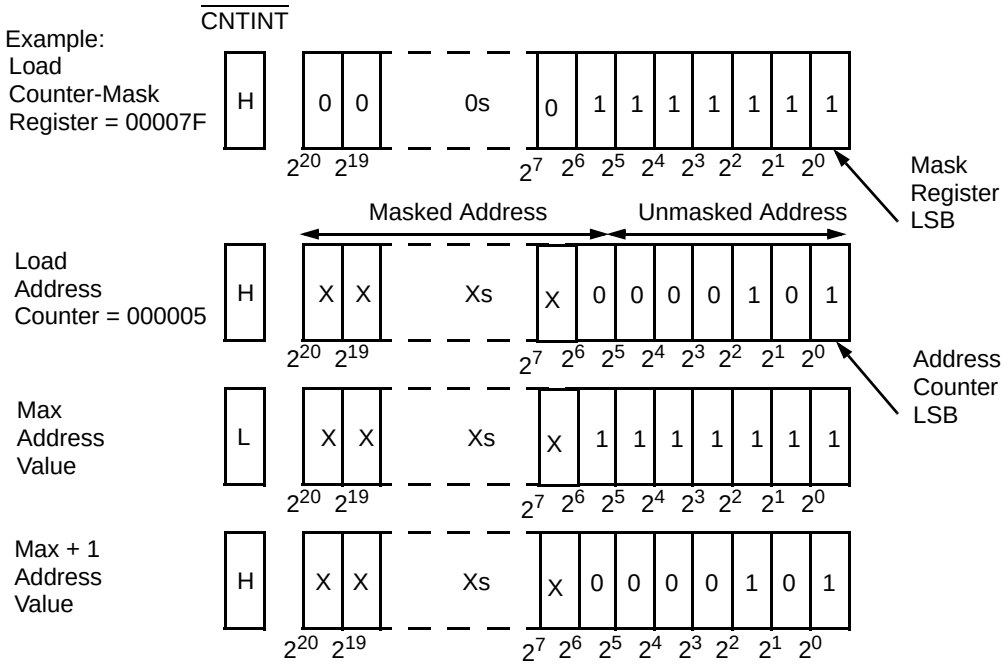


Table 8. Interrupt Operation Example

Table 8 shows the interrupt operation example. [1, 20, 22, 23, 24]

Function	Left Port				Right Port			
	$R/\overline{W}_L$	$\overline{CE}_L$	A_{0L-20L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	A_{0R-20R}	$\overline{INT}_R$
Set Right $\overline{INT}_R$ Flag	L	L	Max Address	X	X	X	X	L
Reset Right $\overline{INT}_R$ Flag	X	X	X	X	H	L	Max Address	H
Set Left $\overline{INT}_L$ Flag	X	X	X	L	L	L	Max Address–1	X
Reset Left $\overline{INT}_L$ Flag	H	L	Max Address–1	H	X	X	X	X

Notes
22. $\overline{CE}$ is internal signal. $\overline{CE}$ = LOW if $\overline{CE}_0$ = LOW and CE_1 = HIGH. For a single read operation, $\overline{CE}$ only needs to be asserted once at the rising edge of the C and is deasserted after that. Data is out after the following C edge and is tri-stated after the next C edge.
23. $\overline{OE}$ is "Don't Care" for mailbox operation.
24. At least one of $\overline{BE0}$, $\overline{BE1}$, $\overline{BE2}$, $\overline{BE3}$, $\overline{BE4}$, $\overline{BE5}$, $\overline{BE6}$, or $\overline{BE7}$ must be LOW.
25. The "X" in this diagram represents the counter's upper bits.

Master Reset

The FullFlex family of Dual Ports undergoes a complete reset when MRST is asserted. MRST must be driven by $VDDIO_L$ referenced levels. The MRST is asserted asynchronously to the clocks and must remain asserted for at least t_{RS}. When asserted MRST deasserts READY, initializes the internal burst counters, internal mirror registers, and internal busy addresses to zero. It also initializes the internal mask register to all 1s. All mailbox interrupts (INT), busy address outputs (BUSY), and burst counter interrupts (CNTINT) are deasserted upon master reset. Additionally, do not release MRST until all power supplies including VREF are fully ramped and all port clocks and mode select inputs (LOWSPD, ZQ, CQEN, FTSEL, and PORTSTD) are valid and stable. This begins calibration of the DLL and VIM circuits. READY is asserted within 1024 clock cycles. READY is a wired OR capable output with a strong pull up and weak pull down. Up to four outputs may be connected together. For faster pull down of the signal, connect a 250 Ohm resistor to VSS. If the DLL and VIM circuits are disabled for a port, the port is operational within five clock cycles. However, the READY is asserted within 160 clock cycles.

IEEE 1149.1 Serial Boundary Scan (JTAG)

The FullFlex families incorporate an IEEE 1149.1 serial boundary scan test access port (TAP). The TAP operates using JEDEC-standard 3.3V or 2.5V IO logic levels depending on the VTTL power supply. It is composed of four input connections and one output connection required by the test logic defined by the standard.

Table 9. JTAG IDCODE Register Definitions

Part Number	Configuration	Value
CYD36S72V18	512Kx72	0C026069h (x2)
CYD36S36V18	1024Kx36	0C023069h
CYD36S18V18	2048Kx36	0C024069h
CYD18S72V18	256Kx72	0C025069h
CYD18S36V18	512Kx36	0C026069h
CYD18S18V18	1024Kx18	0C027069h
CYD09S72V18	128Kx72	0C028069h
CYD09S36V18	256Kx36	0C029069h
CYD09S18V18	512Kx18	0C02A069h
CYD04S72V18	64Kx72	0C02B069h
CYD04S36V18	128Kx36	0C02C069h
CYD04S18V18	256Kx18	0C02D069h
CYD02S36V18	64Kx36	0C030069h

Table 10.Scan Registers Sizes

Register Name	Bit Size
Instruction	4
Bypass	1
Identification	32
Boundary Scan	n[26]

Table 11.Instruction Identification Codes

Instruction	Code	Description
EXTEST	0000	Captures the input and output ring contents. Places the BSR between the TDI and TDO.
BYPASS	1111	Places the BYR between TDI and TDO.
IDCODE	1011	Loads the IDR with the vendor ID code and places the register between TDI and TDO.
HIGHZ	0111	Places BYR between TDI and TDO. Forces all FullFlex72 and FullFlex36 output drivers to a High-Z state.
CLAMP	0100	Controls boundary to 1 or 0. Places BYR between TDI and TDO.
SAMPLE/PRELOAD	1000	Captures the input and output ring contents. Places BSR between TDI and TDO.
RESERVED	All other codes	Other combinations are reserved. Do not use other than the mentioned combinations.

Note
26. Details of the boundary scan length is found in the BSDL file for the device.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65°C to + 150°C

Ambient Temperature with Power Applied ..... –55°C to + 125°C

Supply Voltage to Ground Potential.....–0.5V to + 4.1V

DC Voltage Applied to Outputs in High-Z State ..... –0.5V to V_{DDIO} + 0.5V

DC Input Voltage ..... –0.5V to V_{DDIO} + 0.5V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2200V (JEDEC JESD8-6, JESD8-B)

Latch-up Current..... > 200 mA

Operating Range

Range	Ambient Temperature	VCORE
Commercial	0°C to +70°C	1.8V ± 100 mV 1.5V ± 80 mV
Industrial	–40°C to +85°C	1.8V ± 100 mV 1.5V ± 80 mV

Power Supply Requirements

	Min	Typ	Max
LVTTL VDDIO	3.0V	3.3V	3.6V
2.5V LVCMOS VDDIO	2.3V	2.5V	2.7V
HSTL VDDIO	1.4V	1.5V	1.9V
1.8V LVCMOS VDDIO	1.7V	1.8V	1.9V
3.3V VTTL	3.0V	3.3V	3.6V
2.5V VTTL	2.3V	2.5V	2.7V
HSTL VREF	0.68V	0.75V	0.95V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Configuration	All Speed Bins			Unit
			Min	Typ	Max	
V_{OH}	Output HIGH Voltage (V_{DDIO} = Min, I_{OH} = –8 mA)	LVTTL	2.4[27]			V
	(V_{DDIO} = Min, I_{OH} = –4 mA)	HSTL (DC)[28]	VDDIO – 0.4[27]			V
	(V_{DDIO} = Min, I_{OH} = –4 mA)	HSTL (AC)[28]	VDDIO – 0.5[27]			V
	(V_{DDIO} = Min, I_{OH} = –6 mA)	2.5V LVCMOS	1.7[27]			V
	(V_{DDIO} = Min, I_{OH} = –4 mA)	1.8V LVCMOS	VDDIO – 0.45[27]			V
V_{OL}	Output HIGH Voltage (V_{DDIO} = Min, I_{OL} = 8 mA)	LVTTL			0.4[27]	V
	(V_{DDIO} = Min, I_{OL} = 4 mA)	HSTL(DC)[28]			0.4[27]	V
	(V_{DDIO} = Min, I_{OL} = 4 mA)	HSTL (AC)[28]			0.5[27]	V
	(V_{DDIO} = Min, I_{OL} = 6 mA)	2.5V LVCMOS			0.7[27]	V
	(V_{DDIO} = Min, I_{OL} = 4 mA)	1.8V LVCMOS			0.45[27]	V
V_{IH}	Input HIGH Voltage	LVTTL	2		VDDIO + 0.3	V
		HSTL(DC)[28]	VREF + 0.1		VDDIO + 0.3	V
		2.5V LVCMOS	1.7			V
		1.8V LVCMOS	0.65 x VDDIO			V
V_{IL}	Input LOW Voltage	LVTTL	–0.3		0.8	V
		HSTL(DC)[28]	–0.3		VREF – 0.1	V
		2.5V LVCMOS			0.7	V
		1.8V LVCMOS			0.35 x VDDIO	V

Notes

27. These parameters are met with VIM disabled.
28. The DC specifications are measured under steady state conditions. The AC specifications are measured while switching at speed. AC VIH/VIL in HSTL mode are measured with 1V/ns input edge rates

Electrical Characteristics

Over the Operating Range (continued)

Parameter	Description	Configuration	All Speed Bins			Unit
			Min	Typ	Max	
$\overline{READY}$ V_{OH}	Output HIGH Voltage (V_{DDIO} = Min, I_{OH} = –24 mA)	LVTTL	2.7[27]			V
	(V_{DDIO} = Min, I_{OH} = –12 mA)	HSTL(DC)[28]	VDDIO – 0.4[27]			V
	(V_{DDIO} = Min, I_{OH} = –12 mA)	HSTL (AC)[28]	VDDIO – 0.5[27]			V
	(V_{DDIO} = Min, I_{OH} = –15 mA)	2.5V LVCMOS	2.0[27]			V
	(V_{DDIO} = Min, I_{OH} = –12 mA)	1.8V LVCMOS	VDDIO – 0.45[27]			V
$\overline{READY}$ V_{OL}	Output HIGH Voltage (V_{DDIO} = Min, I_O = 0.12 mA)	LVTTL			0.4[27]	V
	(V_{DDIO} = Min, I_{OL} = 0.12 mA)	HSTL(DC)[28]			0.4[27]	V
	(V_{DDIO} = Min, I_{OL} = 0.12 mA)	HSTL (AC)[28]			0.5[27]	V
	(V_{DDIO} = Min, I_{OL} = 0.15 mA)	2.5V LVCMOS			0.7[27]	V
	(V_{DDIO} = Min, I_{OL} = 0.08 mA)	1.8V LVCMOS			0.45[27]	V
I_{OZ}	Output Leakage Current		–10		10	µA
I_{IX1}	Input Leakage Current Except TDI, TMS, MRST, PORTSTD		–10		10	µA
I_{IX2}	Input Leakage Current TDI, TMS, MRST		–300		10	µA
I_{IX3}	Input Leakage Current PORTSTD		–10		300	µA

Electrical Characteristics

Over the Operating Range

Parameter	Description	Configuration		–200		–167		–133		Unit
				Typ	Max	Typ	Max	Typ	Max	
I_{CC}	Operating Current (V_{CORE} = Max, I_{OUT} = 0 mA) Outputs Disabled	512Kx72	Com.	1440	1800	1280	1620	1120	1430	mA
			Ind.	N/A	N/A	1330	1730	1170	1550	mA
		1024Kx36	Com.	1180	1500	1050	1350	930	1220	mA
			Ind.	N/A	N/A	1110	1470	980	1330	mA
		2048Kx18	Com.	1130	1430	1000	1290	890	1160	mA
			Ind.	N/A	N/A	1060	1410	940	1280	mA
		256Kx72	Com.	800	980	700	880	N/A	N/A	mA
			Ind.	820	1030	730	930	N/A	N/A	mA
		512Kx36	Com.	640	800	570	720	N/A	N/A	mA
			Ind.	670	860	590	780	N/A	N/A	mA
		1024Kx18	Com.	610	770	540	690	N/A	N/A	mA
			Ind.	640	830	570	750	N/A	N/A	mA
		128Kx72	Com.	640	790	560	700	N/A	N/A	mA
			Ind.	660	830	580	740	N/A	N/A	mA
		256Kx36	Com.	540	640	470	570	N/A	N/A	mA
			Ind.	550	670	490	600	N/A	N/A	mA
		512Kx18	Com.	550	660	480	580	N/A	N/A	mA
			Ind.	570	690	500	610	N/A	N/A	mA
		64Kx72	Com.	620	740	540	650	N/A	N/A	mA
			Ind.	630	770	550	680	N/A	N/A	mA
		128Kx36	Com.	510	590	450	520	N/A	N/A	mA
			Ind.	520	600	460	530	N/A	N/A	mA
		256Kx18	Com.	530	610	460	530	N/A	N/A	mA
			Ind.	540	620	470	550	N/A	N/A	mA
		64Kx36	Com.					N/A	N/A	mA
			Ind.					N/A	N/A	mA

Electrical Characteristics

Over the Operating Range (continued)

Parameter	Description	Configuration		–200		–167		–133		Unit
				Typ	Max	Typ	Max	Typ	Max	
I_{SB1}	Standby Current (Both Ports TTL Level) $\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}	512Kx72	Com.	1000	1250	920	1160	830	1060	mA
			Ind.	N/A	N/A	970	1260	880	1170	mA
		1024Kx36	Com.	910	1140	820	1050	740	960	mA
			Ind.	N/A	N/A	880	1160	790	1080	mA
		2048Kx18	Com.	890	1110	810	1030	730	940	mA
			Ind.	N/A	N/A	860	1140	780	1050	mA
		256Kx72	Com.	500	630	460	580	N/A	N/A	mA
			Ind.	530	680	490	630	N/A	N/A	mA
		512Kx36	Com.	460	570	410	530	N/A	N/A	mA
			Ind.	480	630	440	580	N/A	N/A	mA
		1024Kx18	Com.	450	560	410	520	N/A	N/A	mA
			Ind.	470	610	430	570	N/A	N/A	mA
		128Kx72	Com.	400	490	360	450	N/A	N/A	mA
			Ind.	420	540	380	490	N/A	N/A	mA
		256Kx36	Com.	380	440	340	400	N/A	N/A	mA
			Ind.	390	470	360	430	N/A	N/A	mA
		512Kx18	Com.	390	460	350	410	N/A	N/A	mA
			Ind.	410	480	370	440	N/A	N/A	mA
		64Kx72	Com.	380	450	340	400	N/A	N/A	mA
			Ind.	390	480	350	430	N/A	N/A	mA
		128Kx36	Com.	360	400	320	360	N/A	N/A	mA
			Ind.	360	410	330	370	N/A	N/A	mA
		256Kx18	Com.	370	410	320	370	N/A	N/A	mA
			Ind.	370	420	330	380	N/A	N/A	mA
		64Kx36	Com.					N/A	N/A	mA
			Ind.					N/A	N/A	mA

Electrical Characteristics

Over the Operating Range (continued)

Parameter	Description	Configuration		–200		–167		–133		Unit
				Typ	Max	Typ	Max	Typ	Max	
I_{SB2}	Standby Current (One Port TTL or CMOS Level) $\overline{CE}_L \mid \overline{CE}_R \geq V_{IH}$, f = f_{MAX}	512Kx72	Com.	1300	1570	1160	1410	1020	1260	mA
			Ind.	N/A	N/A	1210	1520	1070	1370	mA
		1024Kx36	Com.	1090	1330	980	1210	870	1100	mA
			Ind.	N/A	N/A	1030	1330	920	1210	mA
		2048Kx18	Com.	1040	1270	930	1160	830	1050	mA
			Ind.	N/A	N/A	980	1270	880	1160	mA
		256Kx72	Com.	650	790	580	710	N/A	N/A	mA
			Ind.	680	840	610	760	N/A	N/A	mA
		512Kx36	Com.	550	670	490	610	N/A	N/A	mA
			Ind.	570	730	520	670	N/A	N/A	mA
		1024Kx18	Com.	520	640	470	580	N/A	N/A	mA
			Ind.	550	690	490	640	N/A	N/A	mA
		128Kx72	Com.	520	630	460	560	N/A	N/A	mA
			Ind.	550	670	480	610	N/A	N/A	mA
		256Kx36	Com.	460	530	400	470	N/A	N/A	mA
			Ind.	480	560	430	500	N/A	N/A	mA
		512Kx18	Com.	460	530	410	480	N/A	N/A	mA
			Ind.	480	560	430	510	N/A	N/A	mA
		64Kx72	Com.	500	580	440	510	N/A	N/A	mA
			Ind.	510	610	450	550	N/A	N/A	mA
		128Kx36	Com.	440	480	380	420	N/A	N/A	mA
			Ind.	450	500	390	440	N/A	N/A	mA
		256Kx18	Com.	440	490	390	430	N/A	N/A	mA
			Ind.	450	500	400	450	N/A	N/A	mA
		64Kx36	Com.					N/A	N/A	mA
			Ind.					N/A	N/A	mA

Electrical Characteristics

Over the Operating Range (continued)

Parameter	Description	Configuration		All Speed Bins		Unit
				Typ	Max	
I_{SB3}	Standby Current (Both Ports CMOS Level) CE_L and $CE_R \geq V_{CORE} - 0.2V$, f = 0	512Kx72	Com.	410	590	mA
			Ind.	460	700	mA
		1024Kx36	Com.	410	590	mA
			Ind.	460	700	mA
		2048Kx18	Com.	410	590	mA
			Ind.	460	700	mA
		256Kx72	Com.	210	300	mA
			Ind.	230	350	mA
		512Kx36	Com.	210	300	mA
			Ind.	230	350	mA
		1024Kx18	Com.	210	300	mA
			Ind.	230	350	mA
		128Kx72	Com.	150	200	mA
			Ind.	170	220	mA
		256Kx36	Com.	150	200	mA
			Ind.	170	220	mA
		512Kx18	Com.	150	200	mA
			Ind.	170	220	mA
		64Kx72	Com.	130	150	mA
			Ind.	140	170	mA
		128Kx36	Com.	130	150	mA
			Ind.	140	170	mA
		256Kx18	Com.	130	150	mA
			Ind.	140	170	mA

Table 12.Capacitance

Signals	Packages			
	CYD18S72V18 CYD09S72V18 CYD04S72V18 CYD18S36V18 CYD09S36V18 CYD04S36V18 CYD02S36V18	CYD18S18V18 CYD09S18V18 CYD04S18V18	CYD36S72V18 CYD36S36V18	CYD36S18V18
$\overline{OE}$	12 pF	12 pF	20 pF	20 pF
$\overline{BE}$, DQ	10 pF	18 pF	16 pF	30 pF
All other signals	10 pF	10 pF	16 pF	16 pF

AC Test Load and Waveforms

Figure 9. Output Test Load for LVTTL/CMOS

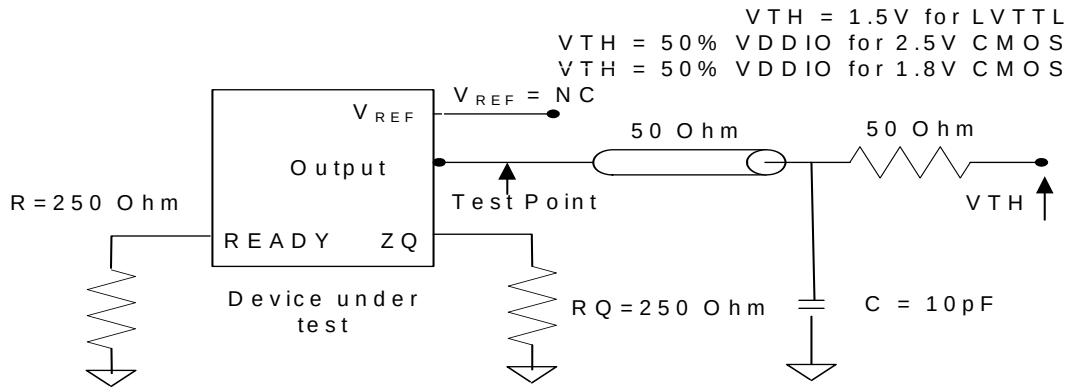


Figure 10. Output Test Load for HSTL

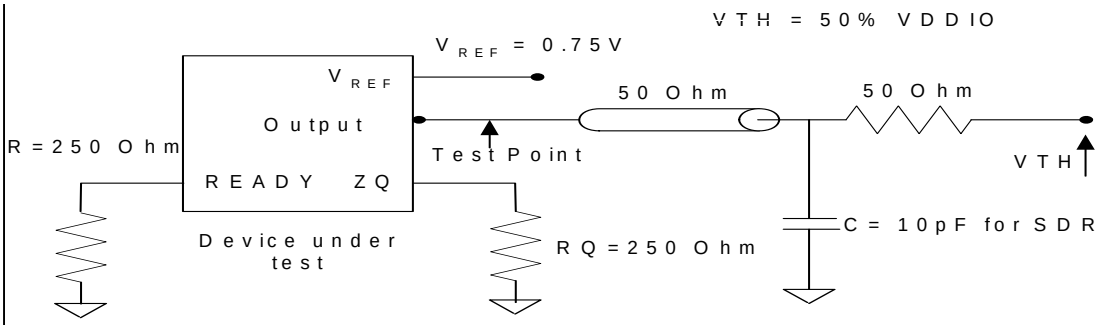
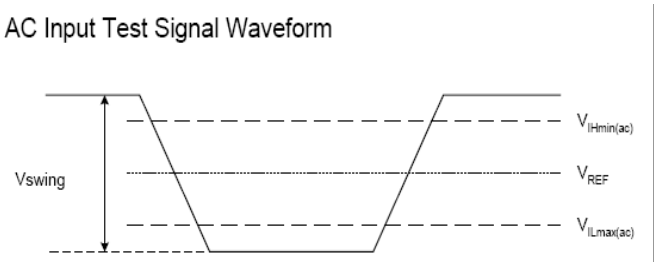


Figure 11. HSTL Input Waveform



Vswing = 1.0V
VREF = 0.75V
V_{IH} = 1.25V
V_{IL} = 0.25V
Slew = 2.0V/ns
All input parameters are referenced to VREF

Switching Characteristics Over the Operating Range

Table 13.SDR Mode, Signals Affected by DLL

Parameter	Description	DLL ON ($\overline{\text{LOWSPD}}$=1)[31]						DLL OFF (LOWSPD=0)[31]		Unit
		–200		–167		–133				
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CD2}[34]	C Rise to DQ Valid for Pipelined Mode		3.30 [30, 33]		4.00 [30, 33]		4.50 [30, 33]		6.00 [30, 33]	ns
t_{CCQ}[34]	C Rise to CQ Rise	1.00	3.30[33]	1.00	4.00[33]	1.00	4.50[33]	1.00	6.00[33]	ns
t_{CKHZ2}[29, 34]	C Rise to DQ Output High Z in Pipelined Mode	1.00	3.30 [30, 33]	1.00	4.00 [30, 33]	1.00	4.50 [30, 33]	1.00	6.00 [30, 33]	ns
t_{CKLZ2}[29, 34]	C Rise to DQ Output Low Z in Pipelined Mode	1.00		1.00		1.00		1.00		ns

Table 14.SDR Mode

Parameter	Description		–200		–167		–133		Unit
			Min	Max	Min	Max	Min	Max	
f_{MAX} (PIPELINED)	Maximum Operating Frequency for Pipelined Mode		100	200	100	167	100	133	MHz
f_{MAX} (FLOW THROUGH)	Maximum Operating Frequency for Flow Through Mode			77		66.7		55.6	MHz
t_{CYC} (PIPELINED)	C Clock Cycle Time for Pipelined Mode		5.00 [33]	10.00	6.00 [33]	10.00	7.00 [33]	10.00	ns
t_{CYC} (FLOW X THROUGH)	C Clock Cycle Time for Flow Through Mode		13.00 [33]		15.00 [33]		18.00 [33]		ns
t_{CKD}	C Clock Duty Time		45	55	45	55	45	55	%
t_{SD}	Data Input Setup Time to C Rise	HSTL 1.8V LVCMOS	1.50 [30, 33]		1.70 [30, 33]		1.80 [30, 33]		ns
		2.5V LVCMOS 3.3V LVTTL	1.75 [30, 33]		1.95 [30, 33]		2.05 [30, 33]		ns
t_{HD}[32]	Data Input Hold Time after C Rise		0.5		0.5		0.5		ns
t_{SAC}	Address and Control Input Setup Time to C Rise	HSTL 1.8V LVCMOS	1.50 [30, 32, 33]		1.70 [30, 32, 33]		1.80 [30, 32, 33]		ns
		2.5V LVCMOS 3.3V LVTTL	1.75 [30, 32, 33]		1.95 [30, 32, 33]		2.05 [30, 32, 33]		ns
t_{HAC}[32]	Address and Control Input Hold Time after C Rise		0.50		0.60		0.70		ns
t_{OE}	Output Enable to Data Valid			4.40 [30,33]		5.00 [30,33]		5.50 [30,33]	ns
t_{OLZ}[29]	$\overline{\text{OE}}$ to Low Z		1.00		1.00		1.00		ns

Notes
29. Parameters specified with the load capacitance in Figure 9 and Figure 10.
30. For the x18 devices, add 200 ps to this parameter in Table 14.
31. Test conditions assume a signal transition time of 2 V/ns.
32. Add 300 ps to this timing for 36M devices.
33. Add 15% to this parameter if a VCORE of 1.5V is used.
34. This parameter assumes input clock cycle to cycle jitter of ± 0ps.

Table 14.SDR Mode (continued)

Parameter	Description		–200		–167		–133		Unit
			Min	Max	Min	Max	Min	Max	
t_{OHZ}[29]	$\overline{OE}$ to High Z		1.00	4.40 [30, 33]	1.00	5.00 [30, 33]	1.00	5.50 [30, 33]	ns
t_{CD1}	C Rise to DQ Valid for Flow Through Mode (LowSPD = 1)			9.00 [30, 33]		11.00 [30, 33]		13.00 [30, 33]	ns
t_{CA1}	C Rise to Address Readback Valid for Flow Through Mode			9.00[33]		11.00[33]		13.00 [33]	ns
t_{CA2}	C Rise to Address Readback Valid for Pipelined Mode			5.00[33]		6.00[33]		7.50[33]	ns
t_{DC}[34]	DQ Output Hold after C Rise		1.00		1.00		1.00		ns
t_{JIT}	Clock Input Cycle to Cycle Jitter			+/- 200		+/- 200		+/- 200	ps
t_{CQHQV}[34]	Echo Clock (CQ) High to Output Valid	HSTL 1.8V LVCMOS		0.70[30]		0.80[30]		0.90[30]	ns
		2.5V LVCMOS 3.3V LVTTL		0.80[30]		0.90[30]		1.00[30]	ns
t_{CQHQX}[34]	Echo Clock (CQ) High to Output Hold	HSTL 1.8V LVCMOS	–0.70		–0.80		–0.90		ns
		2.5V LVCMOS 3.3V LVTTL	–0.85		–0.95		–1.05		ns
t_{CKHZ1}[29]	C Rise to DQ Output High Z in Flow Through Mode		1.00	9.00 [30, 33]	1.00	11.00 [30, 33]	1.00	13.00 [30, 33]	ns
t_{CKLZ1}[29]	C Rise to DQ Output Low Z in Flow Through Mode		1.00		1.00		1.00		ns
t_{AC}	Address Output Hold after C Rise		1.00		1.00		1.00		ns
t_{CKHZA1}[29]	C Rise to Address Output High Z for Flow Through Mode		1.00	9.00[33]	1.00	11.00 [33]	1.00	13.00 [33]	ns
t_{CKHZA2}[29]	C Rise to Address Output High Z for Pipelined Mode		1.00	5.00[33]	1.00	6.00[33]	1.00	7.50[33]	ns
t_{CKLZA}[29]	C Rise to Address Output Low Z		1.00		1.00		1.00		ns
t_{SCINT}	C Rise to $\overline{CNTINT}$ Low		1.00	3.30[33]	1.00	4.00[33]	1.00	4.50[33]	ns
t_{RCINT}	C Rise to $\overline{CNTINT}$ High		1.00	3.30[33]	1.00	4.00[33]	1.00	4.50[33]	ns
t_{SINT}	C Rise to $\overline{INT}$ Low		0.50	7.00[33]	0.50	8.00[33]	0.50	8.50[33]	ns
t_{RINT}	C Rise to $\overline{INT}$ High		0.50	7.00[33]	0.50	8.00[33]	0.50	8.50[33]	ns
t_{BSY}	C Rise to $\overline{BUSY}$ Valid		1.00	3.30[33]	1.00	4.00[33]	1.00	4.50[33]	ns

Table 15.Master Reset Timing

Parameter	Description	–200		–167		–133		Unit
		Min	Max	Min	Max	Min	Max	
t_{PUP}	Power Up Time	1		1		1		ms
t_{RS}	Master Reset Pulse Width	5		5		5		cycles
t_{RSR}	Master Reset Recovery Time	5		5		5		cycles
t_{RSF}	Master Reset to Outputs Inactive/Hi Z		15		18		22.50	ns
t_{RDY}[35]	Master Reset Release to Port Ready		1024		1024		1024	cycles
t_{CORDY}[36]	C Rise to Port Ready		9.5[33]		11[33]		13[33]	ns

Table 16.JTAG Timing

Parameter	Description	–200		–167		–133		Unit
		Min	Max	Min	Max	Min	Max	
f_{JTAG}	JTAG TAP Controller Frequency		20		20		20	MHz
t_{TCYC}	TCK Cycle Time	50		50		50		ns
t_{TH}	TCK High Time	20		20		20		ns
t_{TL}	TCK Low Time	20		20		20		ns
t_{TMSS}	TMS Setup to TCK Rise	10		10		10		ns
t_{TMSH}	TMS Hold to TCK Rise	10		10		10		ns
t_{TDIS}	TDI Setup to TCK Rise	10		10		10		ns
t_{TDIH}	TDI Hold to TCK Rise	10		10		10		ns
t_{TDOV}	TCK Low to TDO Valid		10		10		10	ns
t_{TDOX}	TCK Low to TDO Invalid	0		0		0		ns
t_{JXZ}	TCK Low to TDO High Z		15		15		15	ns
t_{JZX}	TCK Low to TDO Active		15		15		15	ns
t_{JZX}	TCK Low to TDO Active		15		15		15	ns

.

Notes
35. $\overline{READY}$ is a wired OR capable output with a weak pull down. For a decreased falling delay, connect a 250-Ω resistor to VSS.
36. Add this propagation delay after t_{RDY} for all Master Reset Operations

Switching Waveforms

Figure 12. JTAG Timing

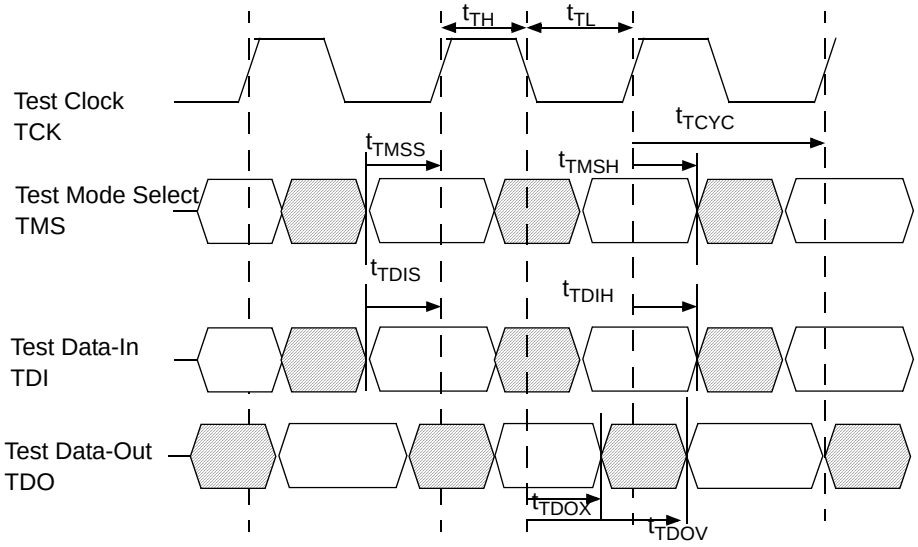
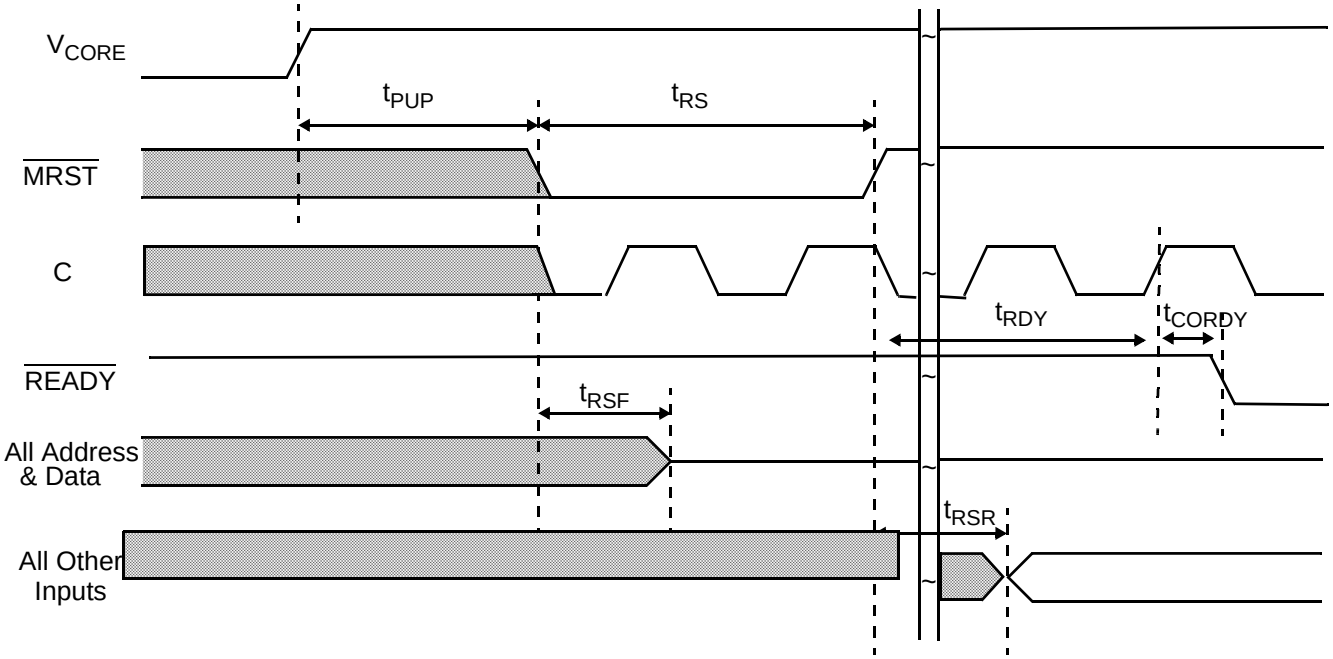


Figure 13. Master Reset [35]



Switching Waveforms (continued)

Figure 14. READ Cycle for Pipelined Mode

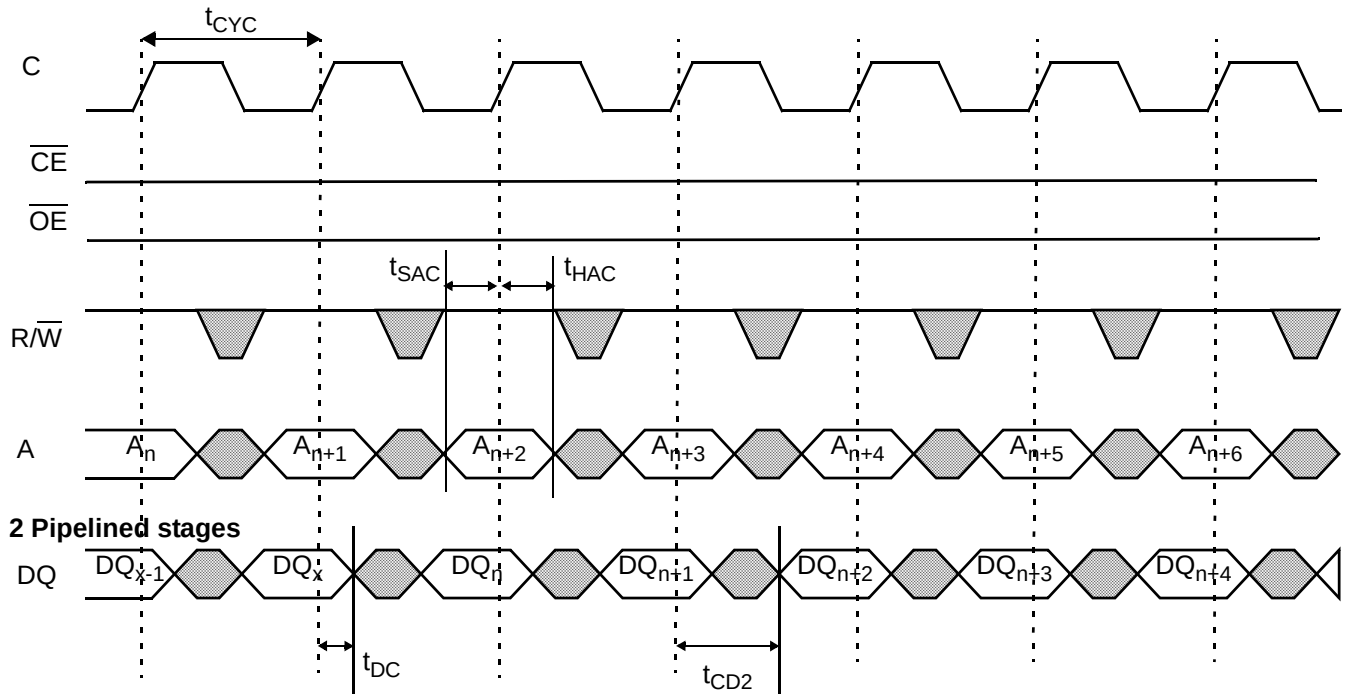
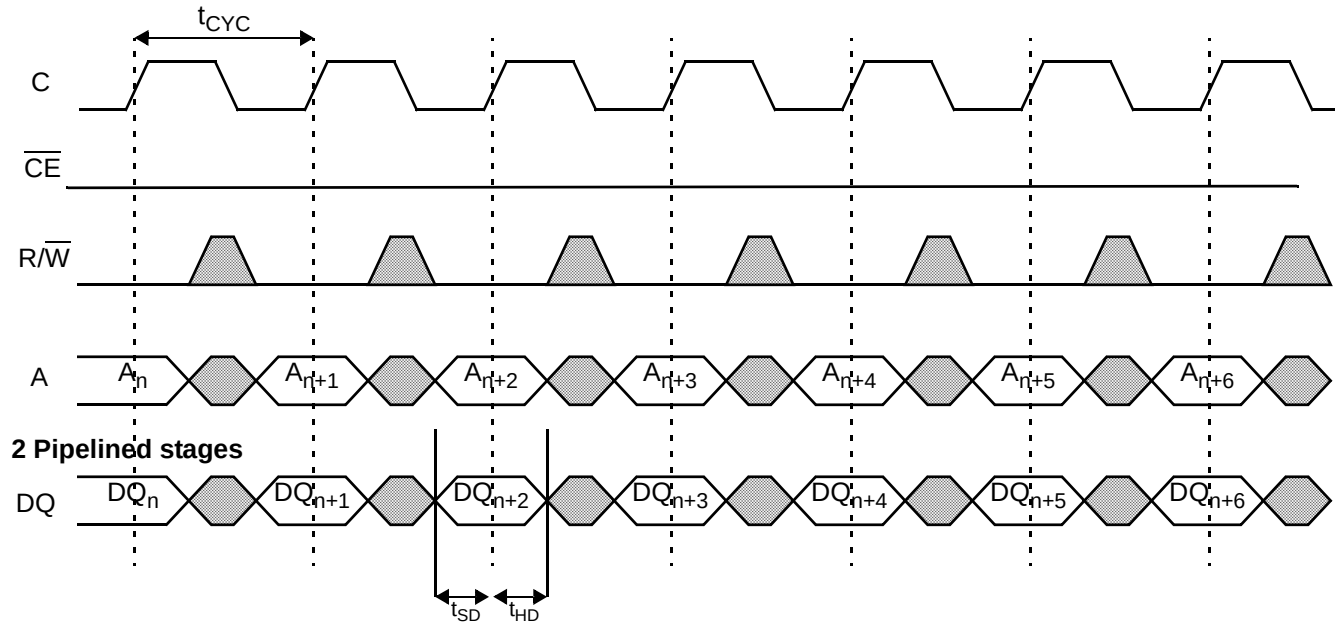


Figure 15. WRITE Cycle for Pipelined and Flow Through Modes



Switching Waveforms (continued)

Figure 16. READ with Address Counter Advance for Pipelined Mode

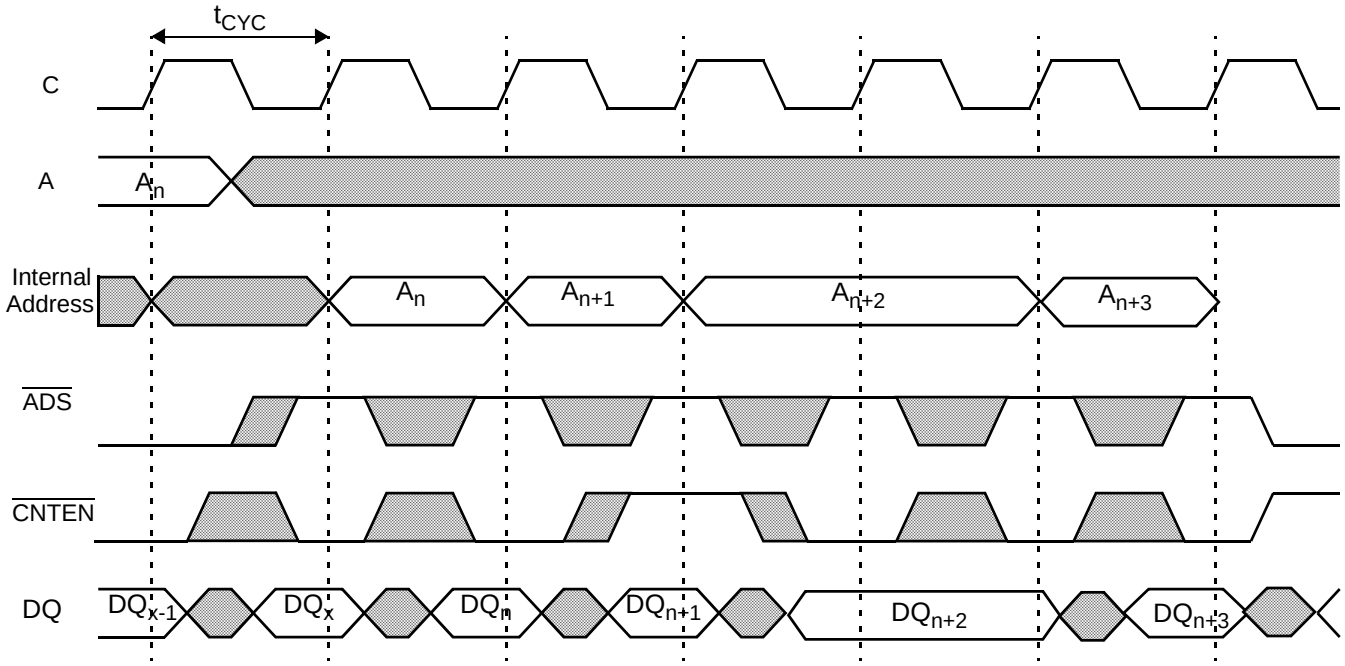
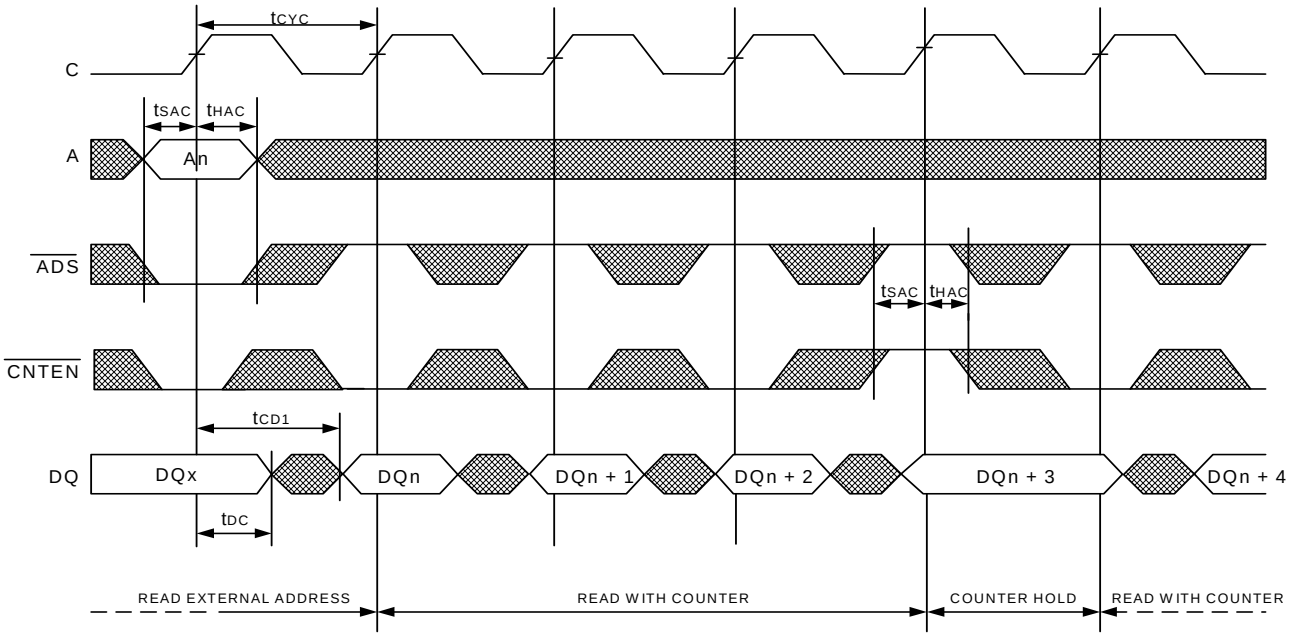


Figure 17. READ with Address Counter Advance for Flow Through Mode



Switching Waveforms (continued)

Figure 18. Port-to-Port WRITE–READ for Pipelined Mode

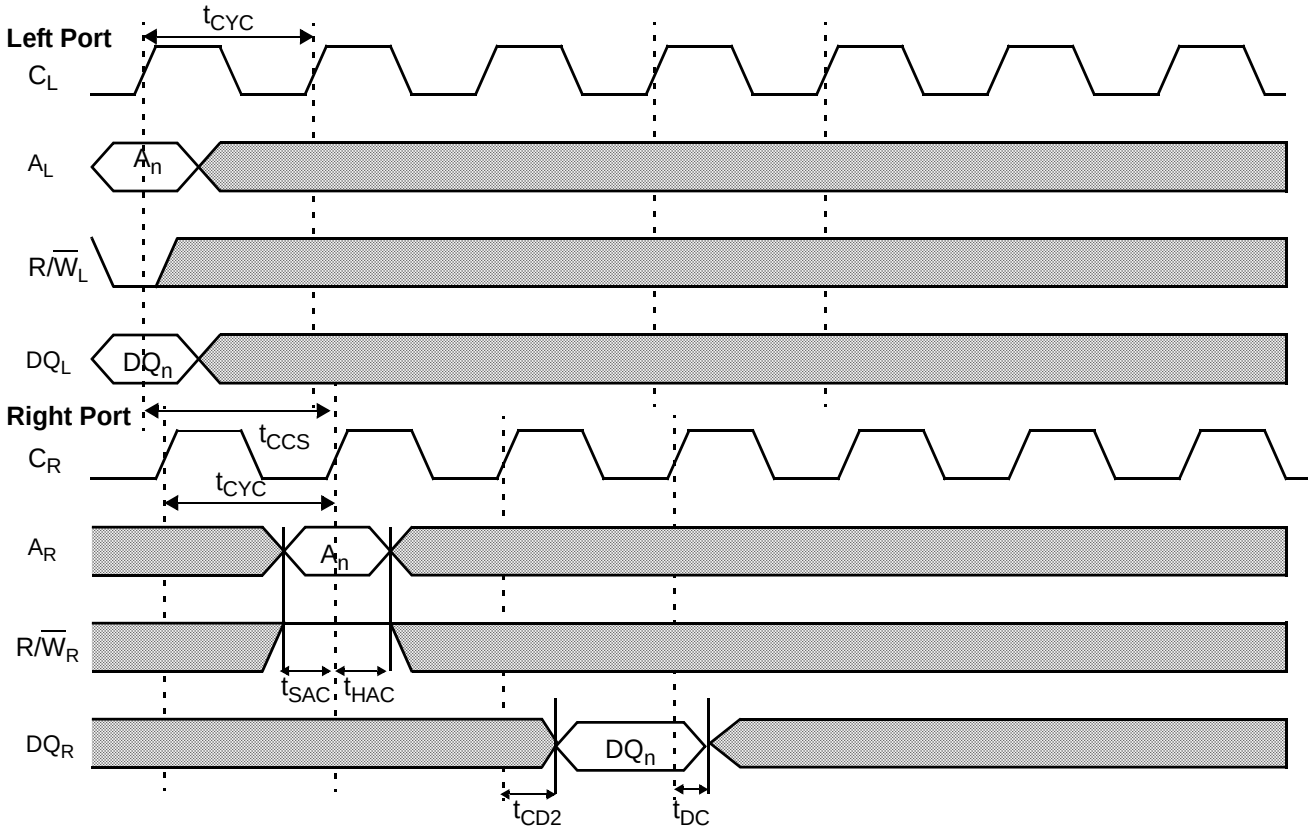
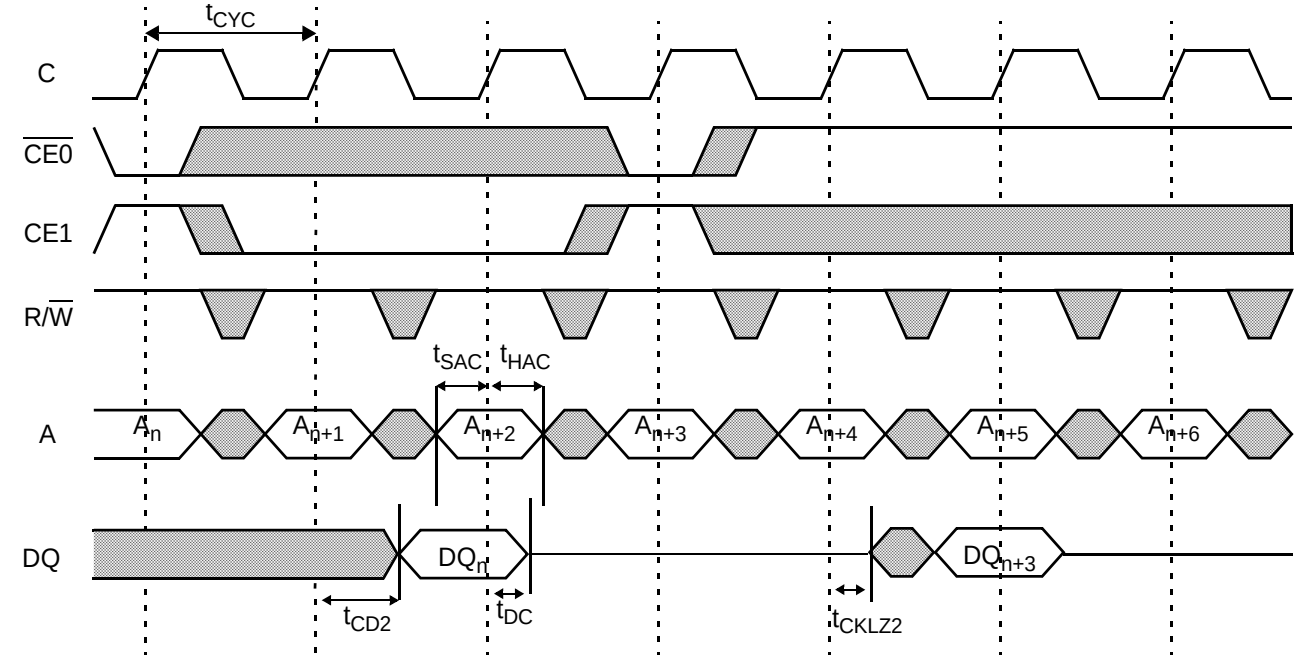


Figure 19. Chip Enable READ for Pipelined Mode



Switching Waveforms (continued)

Figure 20. OE Controlled WRITE for Pipelined Mode

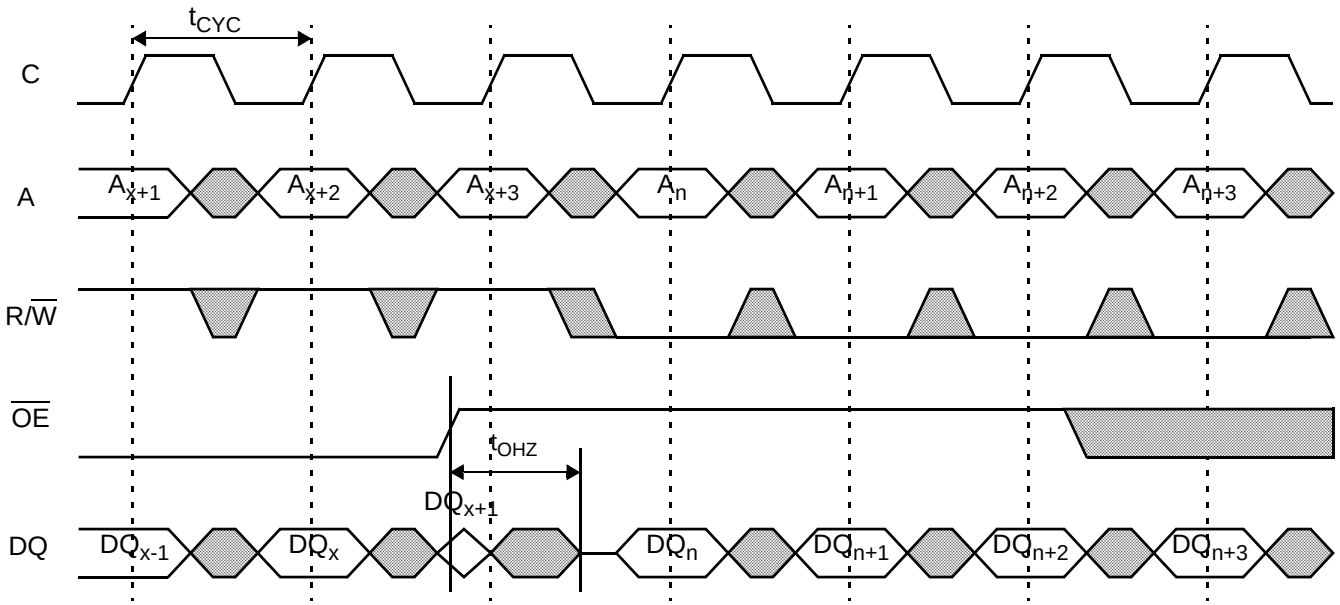
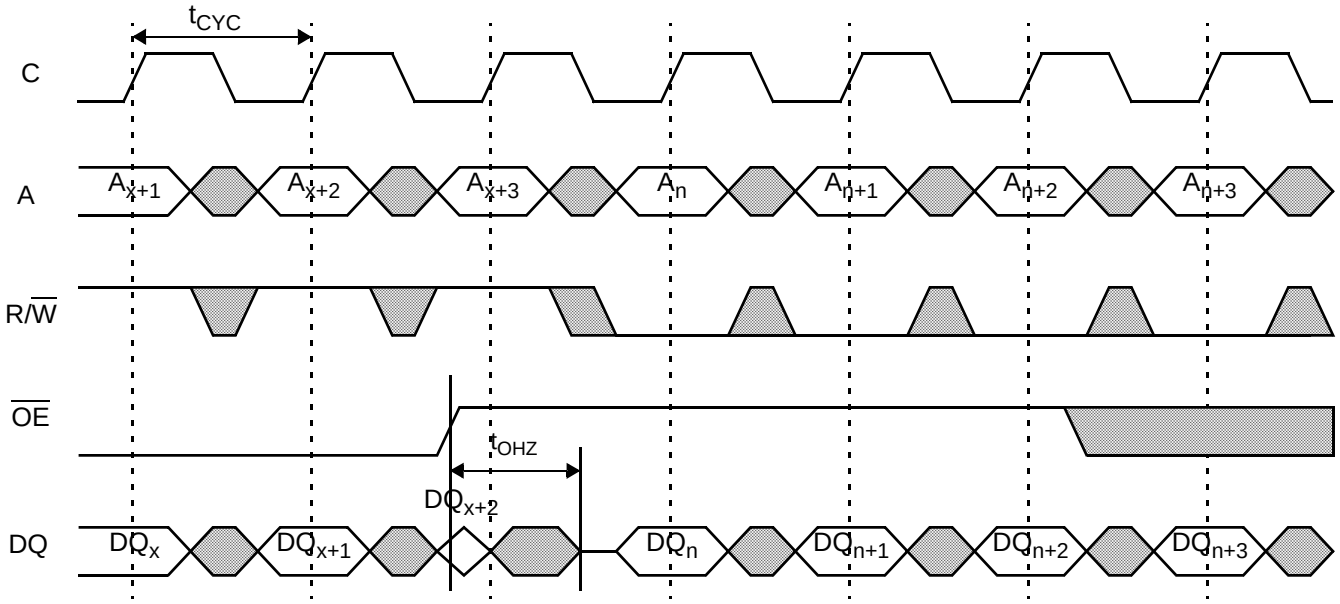
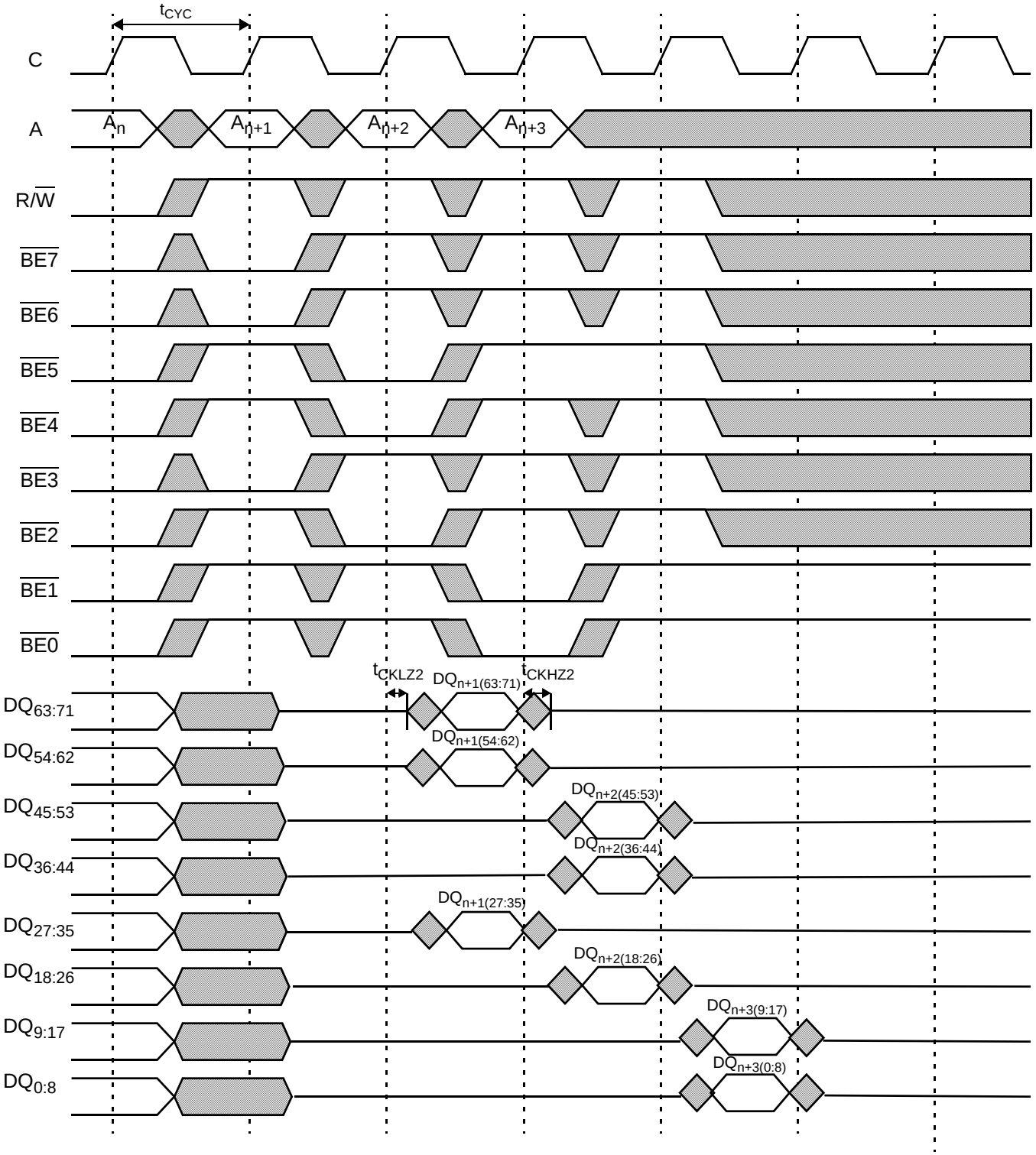


Figure 21. OE Controlled WRITE for Flow Through Mode



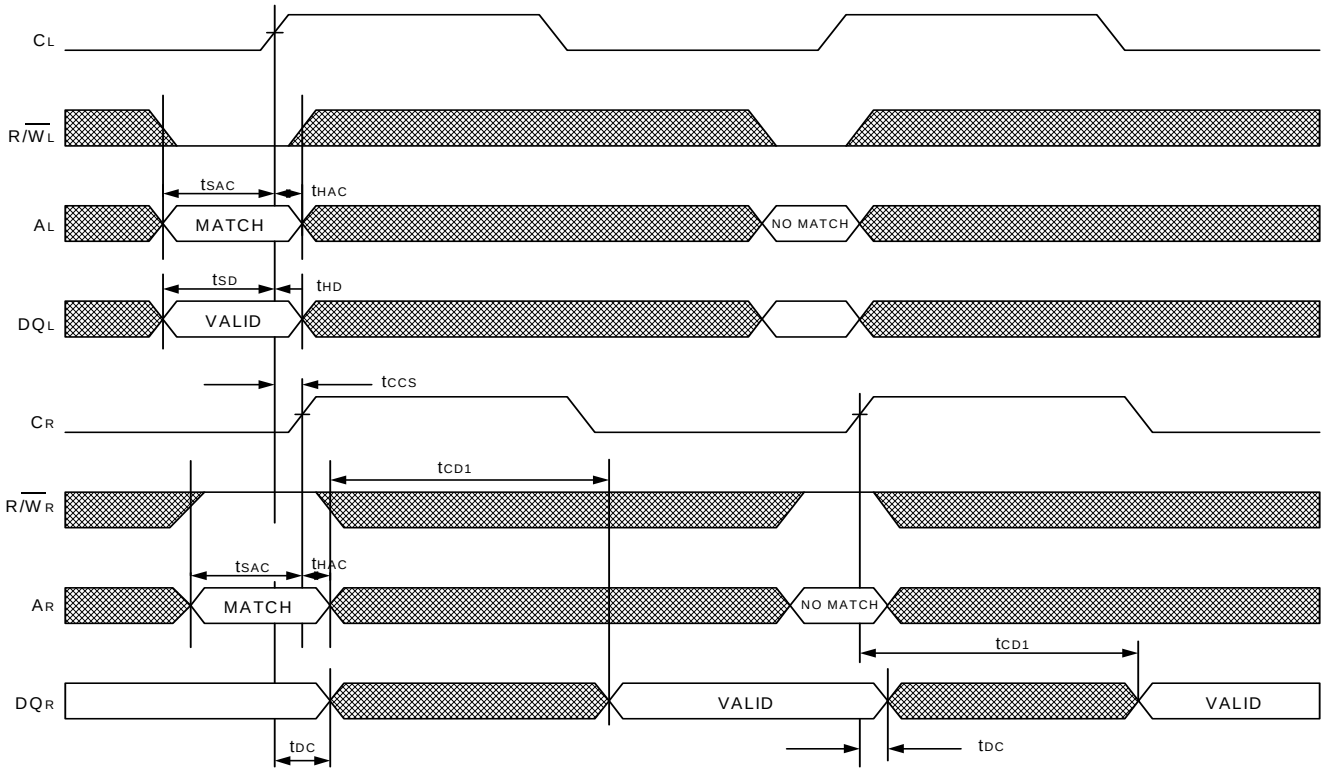
Switching Waveforms (continued)

Figure 22. Byte-Enable READ for Pipelined Mode



Switching Waveforms (continued)

Figure 23. Port-to-Port WRITE-to-READ for Flow Through Mode



Switching Waveforms (continued)

Figure 24. Busy Address Readback for Pipelined and Flow Through Modes, CNT/$\overline{MSK}$ = $\overline{RET}$ = LOW[37]

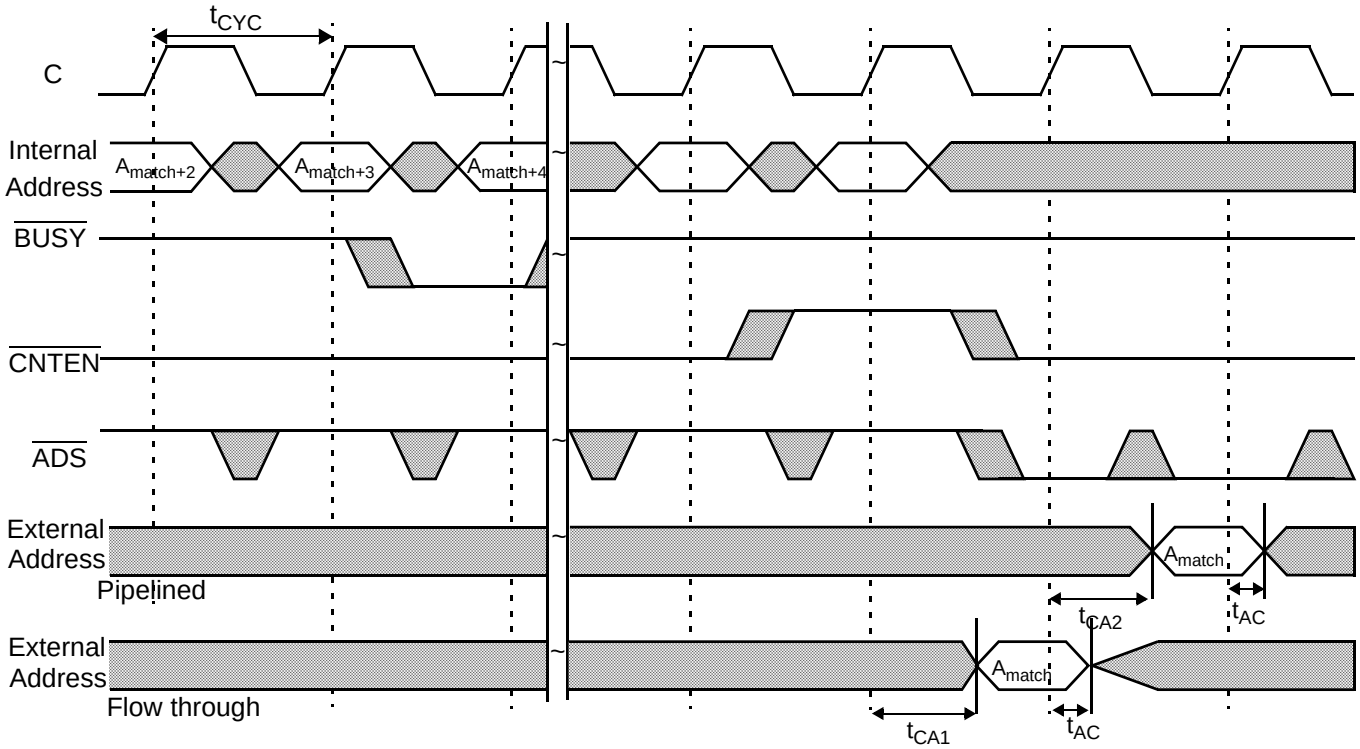
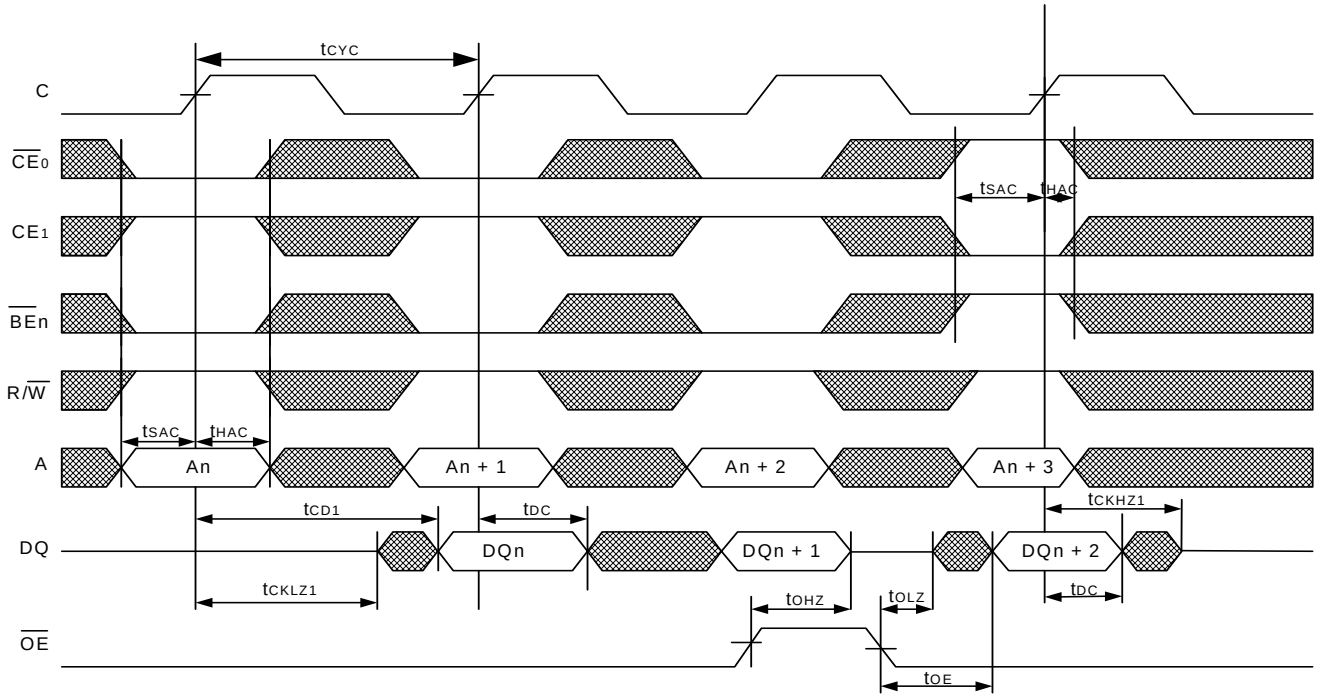


Figure 25. Read Cycle for Flow Through Mode



Note

37. A_{match} is the matching address that is reported on the address bus of the losing port. The counter operation selected for reporting the address is “Busy Address Readback.”

Switching Waveforms (continued)

Figure 26. READ-to-WRITE for Pipelined Mode ($\overline{OE}$ = V_{IL})[38, 39, 40]

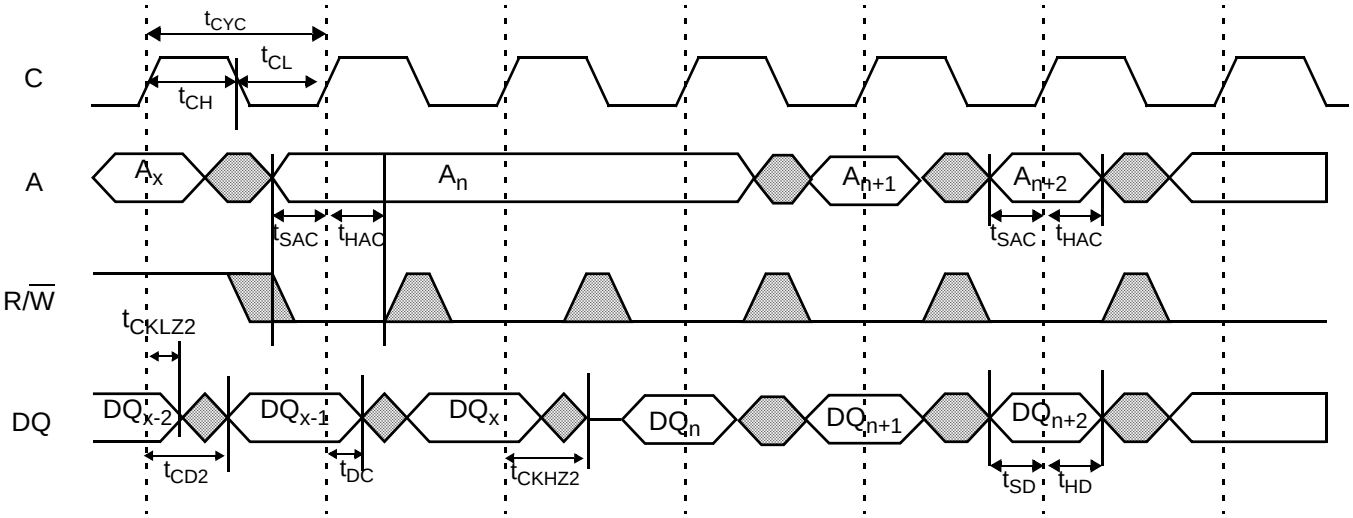
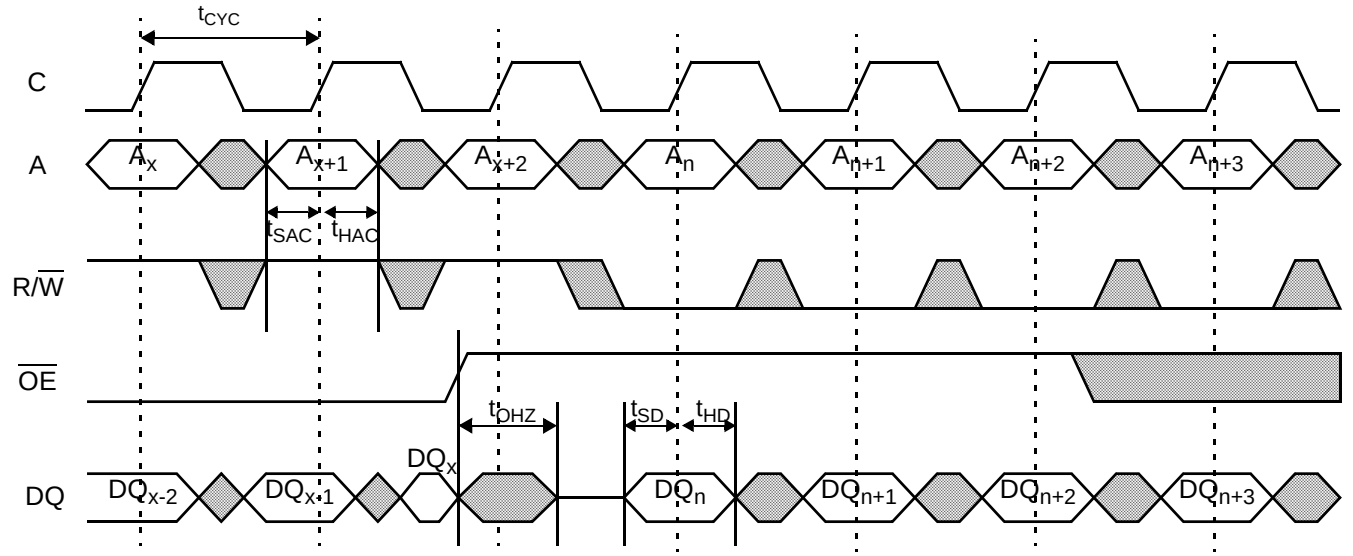


Figure 27. READ-to-WRITE for Pipelined Mode ($\overline{OE}$ Controlled)[41, 42]

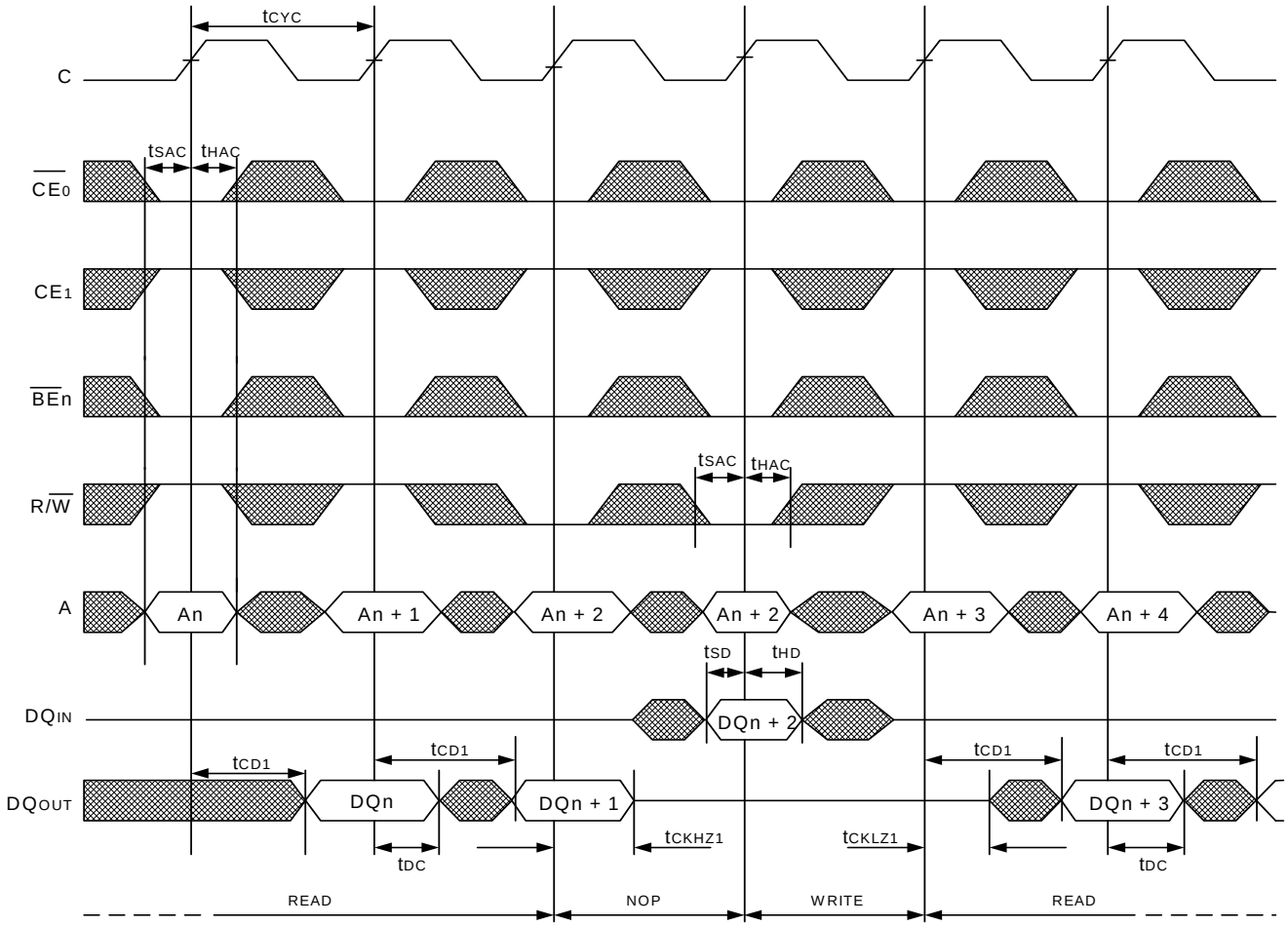


Notes

38. When $\overline{OE}$ = V_{IL}, the last read operation is enabled to complete before the DQ bus is tri-stated and the user is enabled to drive write data.
39. Two dummy writes are issued to accomplish bus turnaround. The third instruction is the first valid write.
40. Chip enable or all byte enables are held inactive during the two dummy writes to avoid data corruption.
41. $\overline{OE}$ is deasserted and t_{OHZ} enabled to elapse before the first write operation is issued.
42. Any write scheduled to complete after $\overline{OE}$ is deasserted is pre-empted.

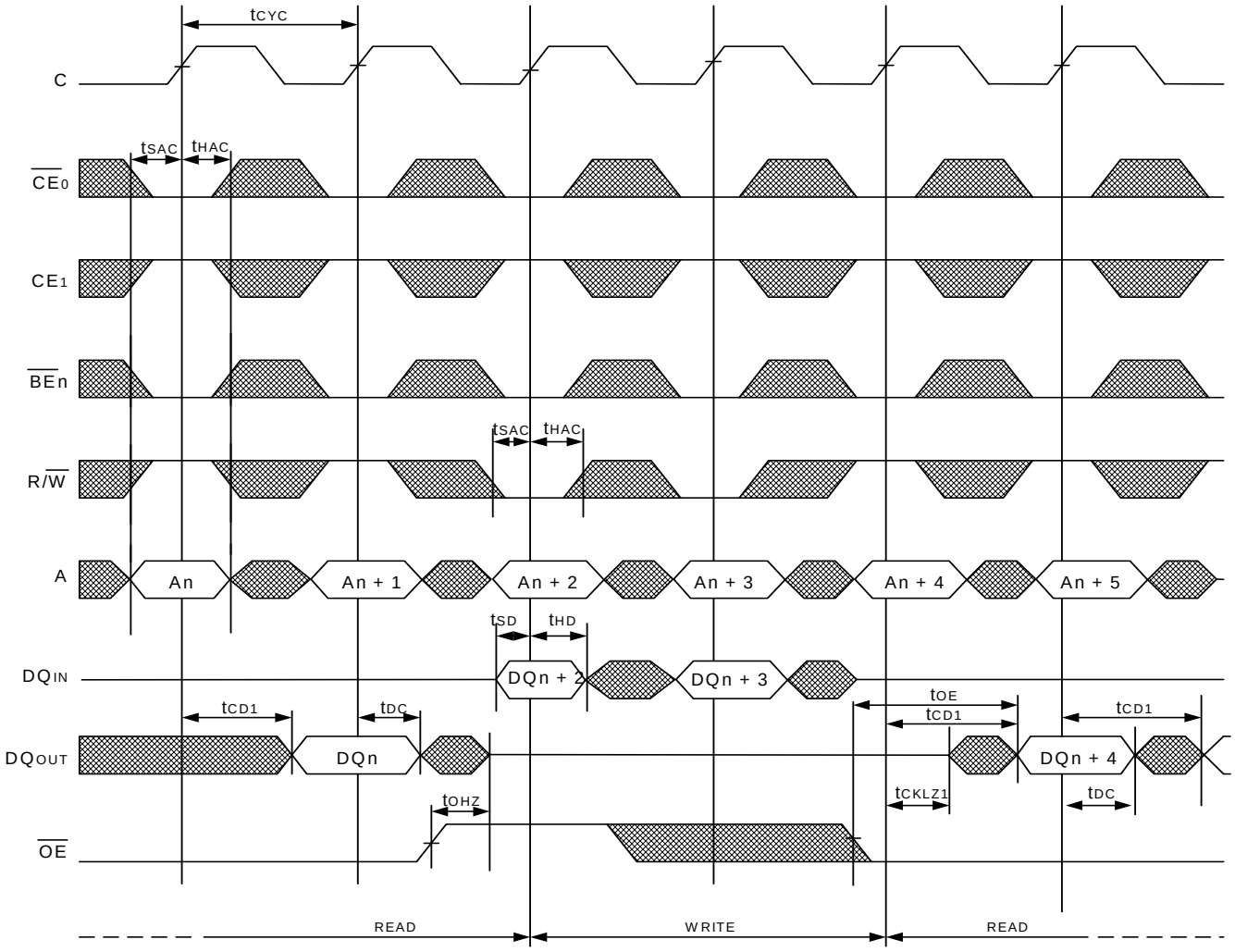
Switching Waveforms (continued)

Figure 28. Read-to-Write-to-Read for Flow Through Mode ($\overline{OE}$ = LOW)



Switching Waveforms (continued)

Figure 29. Read-to-Write-to-Read for Flow Through Mode ($\overline{OE}$ Controlled)



Switching Waveforms (continued)

Figure 30. $\overline{BUSY}$ Timing, WRITE-WRITE Collision for Pipelined and Flow Through Modes, Clock Timing Violates t_{CCS}. (Flag Both Ports)

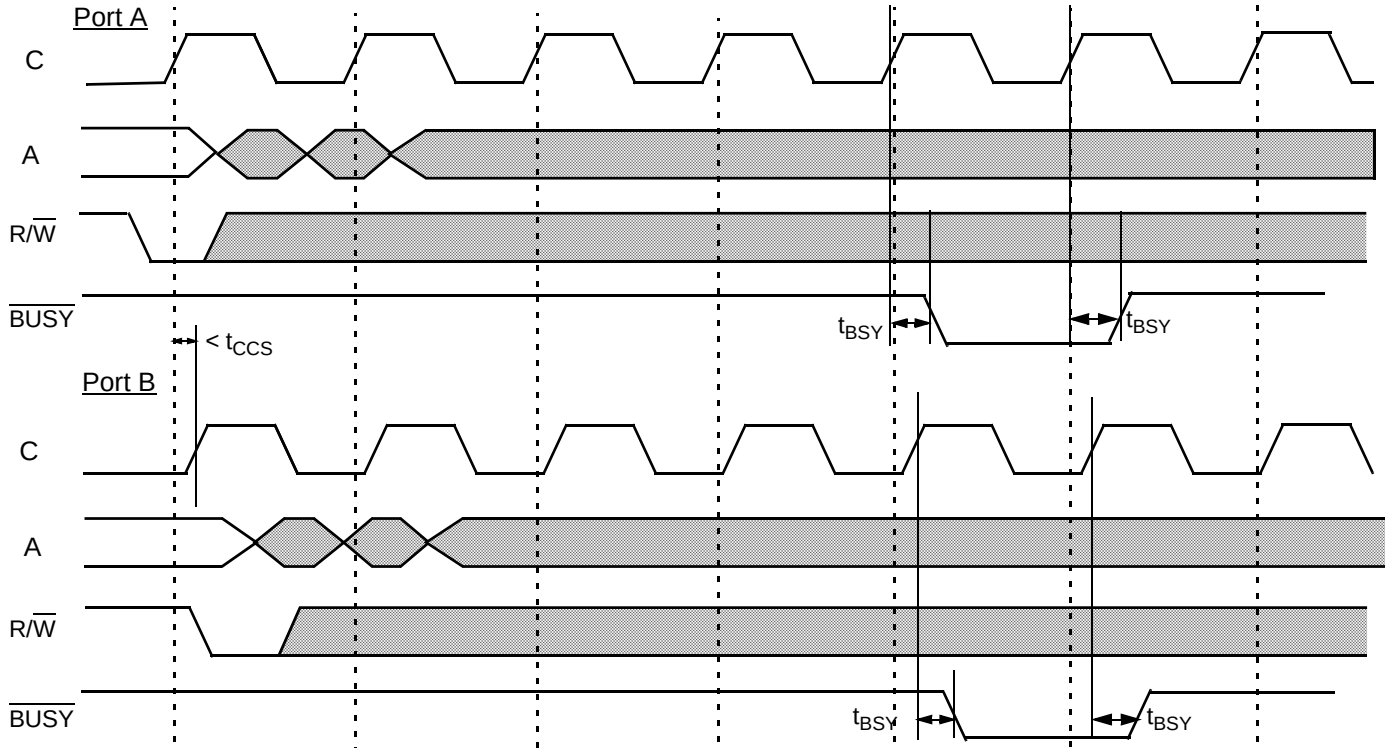
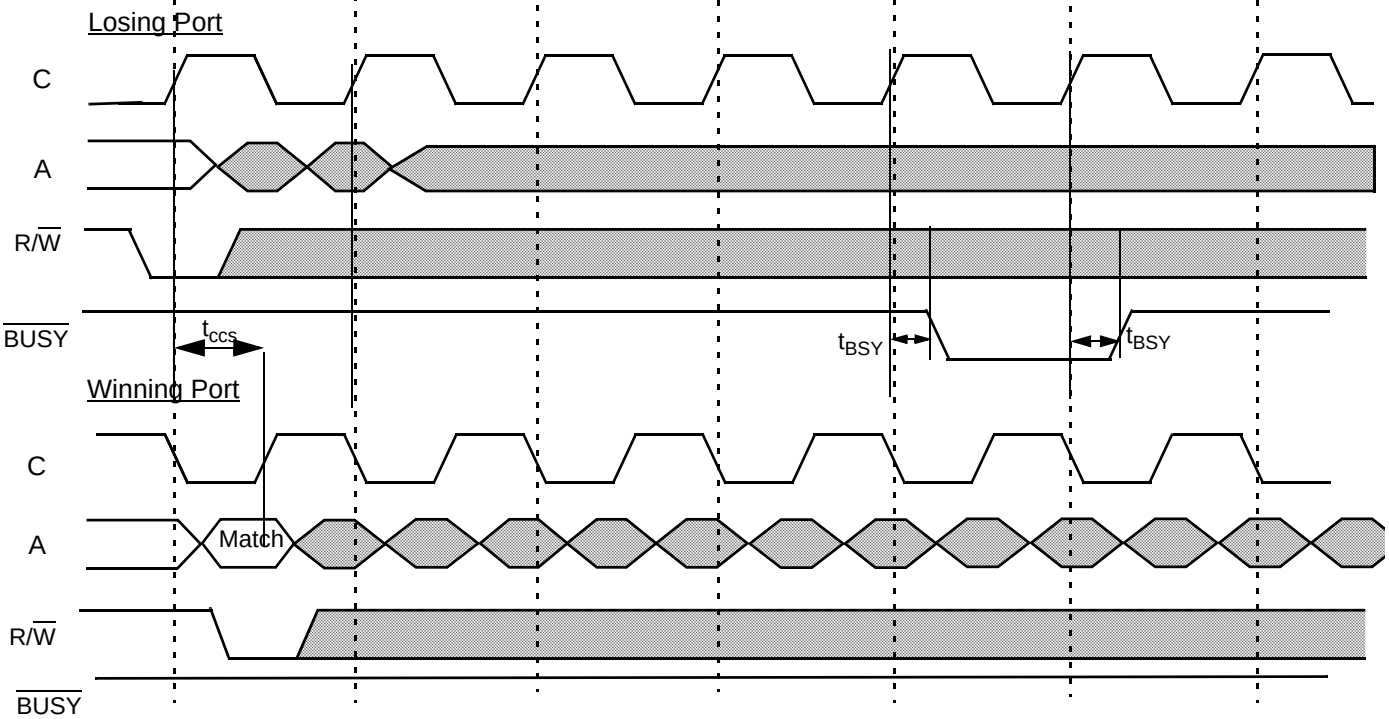
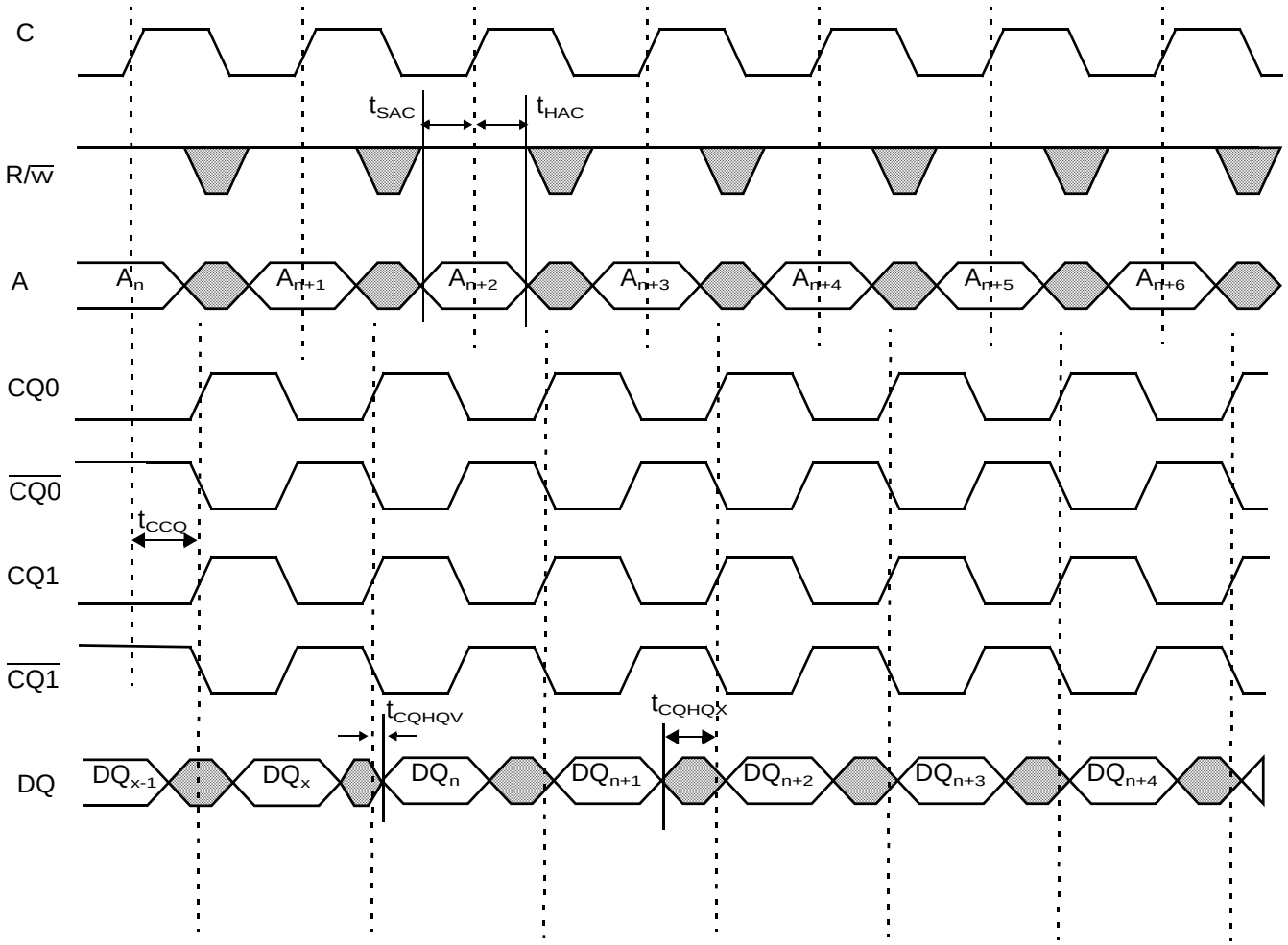


Figure 31. $\overline{BUSY}$ Timing, WRITE-WRITE Collision for Pipelined and Flow Through Modes, Clock Timing Meets t_{CCS}. (Flag Losing Port)



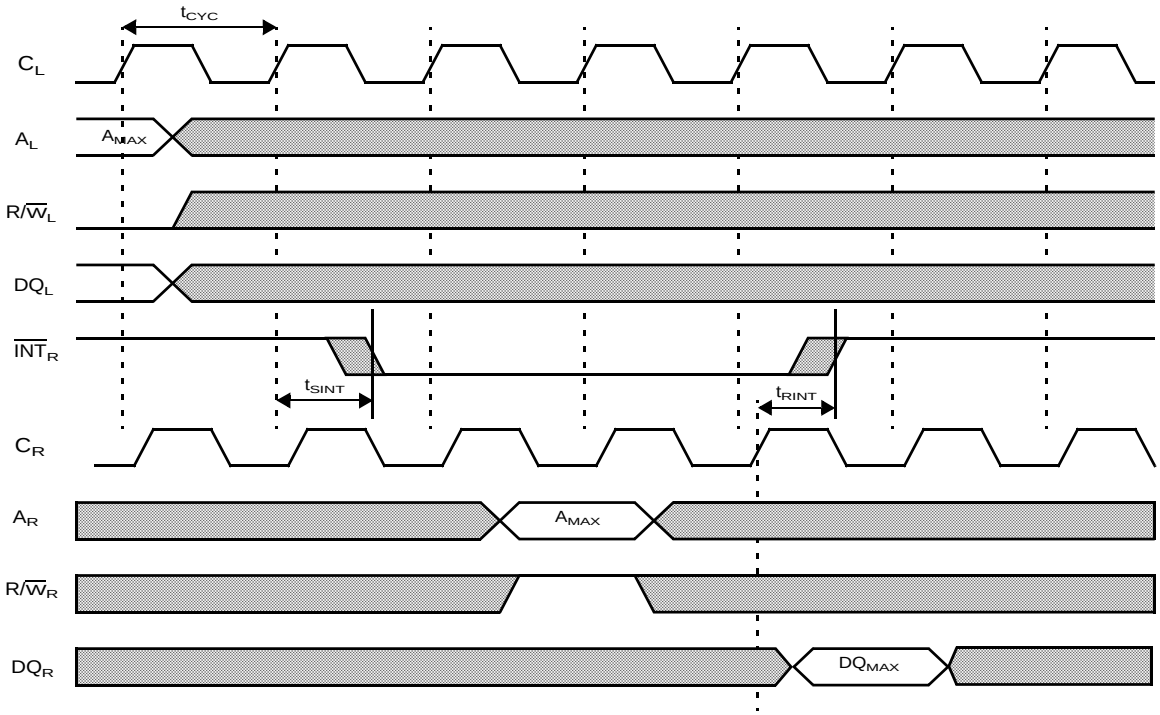
Switching Waveforms (continued)

Figure 32. Read with Echo Clock for Pipelined Mode (CQEN = HIGH)



Switching Waveforms (continued)

Figure 33. Mailbox Interrupt Output



Ordering Information

512K × 72 (36 Mbit) 1.8V/1.5V Synchronous CYD36S72V18 Dual Port SRAM

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
200	CYD36S72V18-200BGXC	001-07825	484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD36S72V18-200BGC		484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch	
167	CYD36S72V18-167BGXC	001-07825	484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD36S72V18-167BGC		484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch	
	CYD36S72V18-167BGXI	001-07825	484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Pb-Free)	Industrial
	CYD36S72V18-167BGI		484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch	
133	CYD36S72V18-133BGXC	001-07825	484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD36S72V18-133BGC		484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch	
	CYD36S72V18-133BGXI	001-07825	484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Pb-Free)	Industrial
	CYD36S72V18-133BGI		484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch	

256K × 72 (18 Mbit) 1.8V/1.5V Synchronous CYD18S72V18 Dual Port SRAM

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
200	CYD18S72V18-200BGXC	51-85218	484-Ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD18S72V18-200BGC		484-Ball Grid Array 23 mm x 23 mm with 1.0 mm pitch	
	CYD18S72V18-200BGXI	51-85218	484-Ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Pb-Free)	Industrial
	CYD18S72V18-200BGI		484-Ball Grid Array 23 mm x 23 mm with 1.0 mm pitch	
167	CYD18S72V18-167BGXC	51-85218	484-Ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD18S72V18-167BGC		484-Ball Grid Array 23 mm x 23 mm with 1.0 mm pitch	
	CYD18S72V18-167BGXI	51-85218	484-Ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Pb-Free)	Industrial
	CYD18S72V18-167BGI		484-Ball Grid Array 23 mm x 23 mm with 1.0 mm pitch	

128K × 72 (9 Mbit) 1.8V/1.5V Synchronous CYD09S72V18 Dual Port SRAM

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
200	CYD09S72V18-200BGXC	51-85218	484-Ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD09S72V18-200BGC		484-Ball Grid Array 23 mm x 23 mm with 1.0 mm pitch	
	CYD09S72V18-200BGXI	51-85218	484-Ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Pb-Free)	Industrial
	CYD09S72V18-200BGI		484-Ball Grid Array 23 mm x 23 mm with 1.0 mm pitch	
167	CYD09S72V18-167BGXC	51-85218	484-Ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD09S72V18-167BGC		484-Ball Grid Array 23 mm x 23 mm with 1.0 mm pitch	
	CYD09S72V18-167BGXI	51-85218	484-Ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Pb-Free)	Industrial
	CYD09S72V18-167BGI		484-Ball Grid Array 23 mm x 23 mm with 1.0 mm pitch	

Ordering Information (continued)

64K × 72 (4 Mbit) 1.8V/1.5V Synchronous CYD04S72V18 Dual Port SRAM

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
200	CYD04S72V18-200BGXC	51-85218	484-Ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD04S72V18-200BGC		484-Ball Grid Array 23 mm x 23 mm with 1.0 mm pitch	
	CYD04S72V18-200BGXI	51-85218	484-Ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Pb-Free)	Industrial
	CYD04S72V18-200BGI		484-Ball Grid Array 23 mm x 23 mm with 1.0 mm pitch	
167	CYD04S72V18-167BGXC	51-85218	484-Ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD04S72V18-167BGC		484-Ball Grid Array 23 mm x 23 mm with 1.0 mm pitch	
	CYD04S72V18-167BGXI	51-85218	484-Ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (Pb-Free)	Industrial
	CYD04S72V18-167BGI		484-Ball Grid Array 23 mm x 23 mm with 1.0 mm pitch	

1024K × 36 (36 Mbit) 1.8V/1.5V Synchronous CYD36S36V18 Dual Port SRAM

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
200	CYD36S36V18-200BGXC	001-07825	484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD36S36V18-200BGC		484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch	
167	CYD36S36V18-167BGXC	001-07825	484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD36S36V18-167BGC		484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch	
	CYD36S36V18-167BGXI	001-07825	484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Pb-Free)	Industrial
	CYD36S36V18-167BGI		484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch	
133	CYD36S36V18-133BGXC	001-07825	484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD36S36V18-133BGC		484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch	
	CYD36S36V18-133BGXI	001-07825	484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Pb-Free)	Industrial
	CYD36S36V18-133BGI		484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch	

512K × 36 (18 Mbit) 1.8V/1.5V Synchronous CYD18S36V18 Dual Port SRAM

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
200	CYD18S36V18-200BBAXC	51-85108	256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD18S36V18-200BBAC		256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch	
	CYD18S36V18-200BBAXI	51-85108	256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Pb-Free)	Industrial
	CYD18S36V18-200BBAI		256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch	
167	CYD18S36V18-167BBAXC	51-85108	256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD18S36V18-167BBAC		256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch	
	CYD18S36V18-167BBAXI	51-85108	256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Pb-Free)	Industrial
	CYD18S36V18-167BBAI		256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch	

Ordering Information (continued)

256K × 36 (9 Mbit) 1.8V/1.5V Synchronous CYD09S36V18 Dual Port SRAM

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
200	CYD09S36V18-200BBXC	51-85108	256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD09S36V18-200BBC		256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch	
	CYD09S36V18-200BBXI	51-85108	256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Pb-Free)	Industrial
	CYD09S36V18-200BBI		256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch	
167	CYD09S36V18-167BBXC	51-85108	256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD09S36V18-167BBC		256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch	
	CYD09S36V18-167BBXI	51-85108	256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Pb-Free)	Industrial
	CYD09S36V18-167BBI		256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch	

128K × 36 (4 Mbit) 1.8V/1.5V Synchronous CYD04S36V18 Dual Port SRAM

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
200	CYD04S36V18-200BBXC	51-85108	256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD04S36V18-200BBC		256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch	
	CYD04S36V18-200BBXI	51-85108	256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Pb-Free)	Industrial
	CYD04S36V18-200BBI		256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch	
167	CYD04S36V18-167BBXC	51-85108	256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD04S36V18-167BBC		256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch	
	CYD04S36V18-167BBXI	51-85108	256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Pb-Free)	Industrial
	CYD04S36V18-167BBI		256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch	

64K × 36 (2 Mbit) 1.8V/1.5V Synchronous CYD02S36V18 Dual Port SRAM

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
200	CYD02S36V18-200BBXI	51-85108	256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Pb-Free)	Industrial
167	CYD02S36V18-167BBXI	51-85108	256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Pb-Free)	Industrial

Ordering Information (continued)

2048K × 18 (36 Mbit) 1.8V/1.5V Synchronous CYD36S18V18 Dual Port SRAM

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
200	CYD36S18V18-200BGXC	001-07825	484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD36S18V18-200BGC		484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch	
167	CYD36S18V18-167BGXC	001-07825	484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD36S18V18-167BGC		484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch	
	CYD36S18V18-167BGXI	001-07825	484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Pb-Free)	Industrial
	CYD36S18V18-167BGI		484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch	
133	CYD36S18V18-133BGXC	001-07825	484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD36S18V18-133BGC		484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch	
	CYD36S18V18-133BGXI	001-07825	484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch (Pb-Free)	Industrial
	CYD36S18V18-133BGI		484-Ball Grid Array 27 mm x 27 mm with 1.0 mm pitch	

1024K × 18 (18 Mbit) 1.8V/1.5V Synchronous CYD18S18V18 Dual Port SRAM

Speed MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
200	CYD18S18V18-200BBAXC	51-85108	256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD18S18V18-200BBAC		256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch	
	CYD18S18V18-200BBAXI	51-85108	256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Pb-Free)	Industrial
	CYD18S18V18-200BBAI		256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch	
167	CYD18S18V18-167BBAXC	51-85108	256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD18S18V18-167BBAC		256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch	
	CYD18S18V18-167BBAXI	51-85108	256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Pb-Free)	Industrial
	CYD18S18V18-167BBAI		256-Ball Grid Array 17 mm x 17mm with 1.0 mm pitch	

512K × 18 (9 Mbit) 1.8V/1.5V Synchronous CYD09S18V18 Dual Port SRAM

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
200	CYD09S18V18-200BBXC	51-85108	256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD09S18V18-200BBC		256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch	
	CYD09S18V18-200BBXI	51-85108	256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Pb-Free)	Industrial
	CYD09S18V18-200BBI		256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch	
167	CYD09S18V18-167BBXC	51-85108	256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD09S18V18-167BBC		256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch	
	CYD09S18V18-167BBXI	51-85108	256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Pb-Free)	Industrial
	CYD09S18V18-167BBI		256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch	

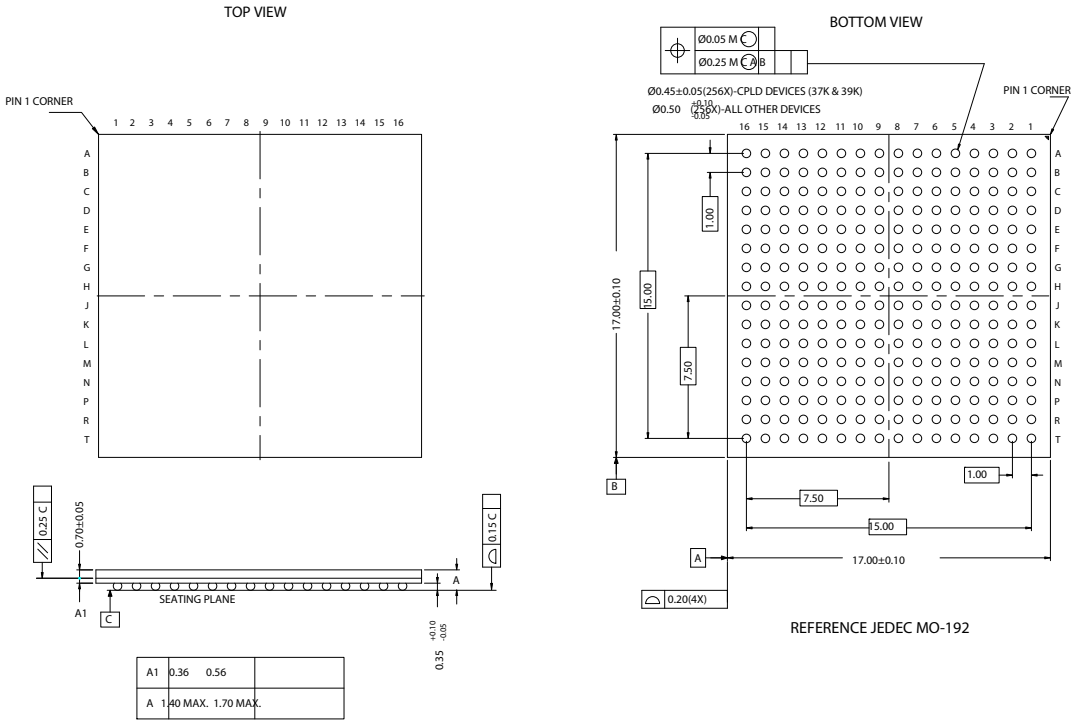
Ordering Information (continued)

256K × 18 (4 Mbit) 1.8V or 1.5V Synchronous CYD04S18V18 Dual Port SRAM

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
200	CYD04S18V18-200BBXC	51-85108	256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD04S18V18-200BBC		256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch	
	CYD04S18V18-200BBXI	51-85108	256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Pb-Free)	Industrial
	CYD04S18V18-200BBI		256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch	
167	CYD04S18V18-167BBXC	51-85108	256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Pb-Free)	Commercial
	CYD04S18V18-167BBC		256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch	
	CYD04S18V18-167BBXI	51-85108	256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (Pb-Free)	Industrial
	CYD04S18V18-167BBI		256-Ball Grid Array 17 mm x 17 mm with 1.0 mm pitch	

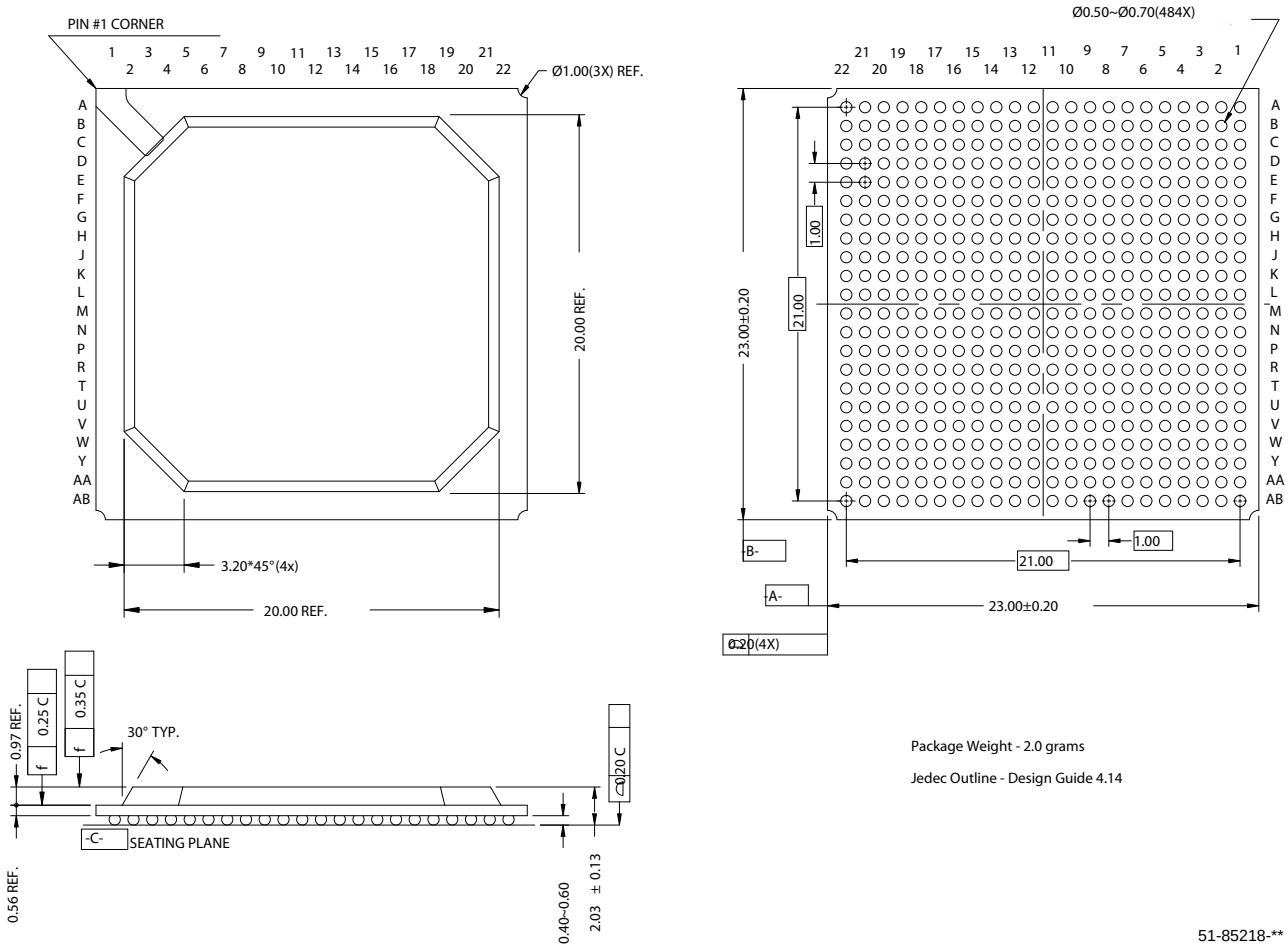
Package Diagrams

Figure 34. 256-Ball FBGA (17 x 17 mm), 51-85108



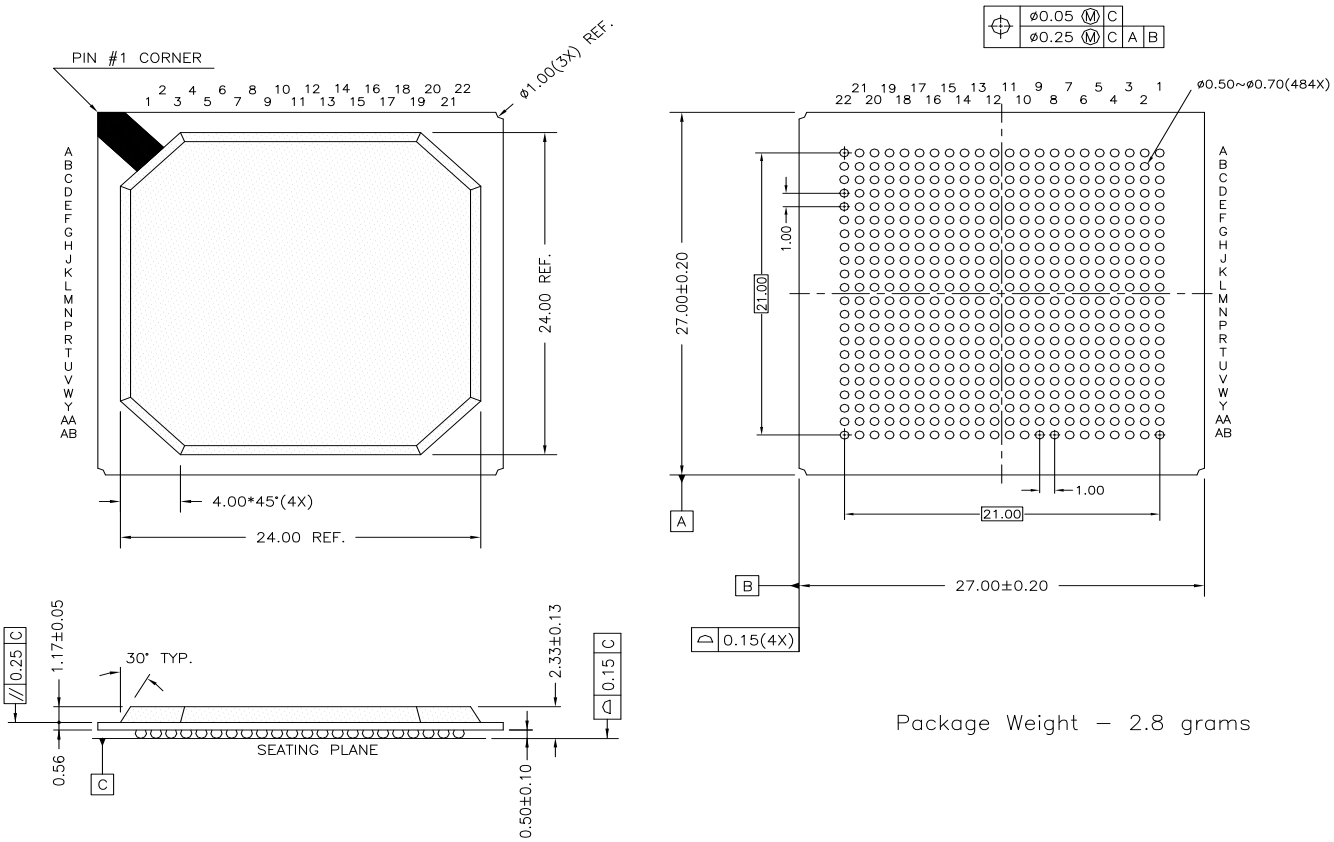
Package Diagrams

Figure 35. 484-Ball PBGA (23 mm x 23 mm x 2.03 mm), 51-85218



Package Diagrams

Figure 36. 484-Ball PBGA (27 mm x 27 mm x 2.33 mm), 001-07825



Document History Page

Document Title: FullFlex™ Synchronous SDR Dual Port SRAM Document Number: 38-06082				
REV.	**ECN NO.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	302411	See ECN	YDT	New data sheet
*A	334036	See ECN	YDT	Corrected typo on page 1 Reproduced PDF file to fix formatting errors
*B	395800	See ECN	SPN	Added statement about no echo clocks for flow through mode Updated electrical characteristics Added note 16 and 17 (1.5V timing) Added note 33 (timing for x18 devices) Updated input edge rate (note 34) Updated table 5 on deterministic access control logic Added description of busy readback in deterministic access control section Changed dummy write descriptions Updated ZQ pins connection details Updated note 24, B0 to BE0 Added power supply requirements to $\overline{MRST}$ and VC_SEL Added note 4 (VIM disable) Updated supply voltage to ground potential to 4.1V Updated parameters on table 15 Updated and added parameters to table 16 Updated x72 pinout to SDR only pinout Updated 484 PBGA pin diagram Updated the pin definition of $\overline{MRST}$ Updated the pin definition of VC_SEL Updated READY description to include Wired OR note Updated master reset to include wired OR note for $\overline{READY}$ Updated minimum V_{OH} value for the 1.8V LVCMOS configuration Updated electrical characteristics to include I_{OH} and I_{OL} values Updated electrical characteristics to include $\overline{READY}$ Added I_{IX3} Updated maximum input capacitance Added Notes 33 and 34Removed Notes 15 and 17 Updated Pin Definitions for CQ0, $\overline{CQ0}$, CQ1, and $\overline{CQ1}$ Removed -100 Speed bin from Table.1 Selection Guide Changed voltage name from V_{DDQ} to V_{DDIO} Changed voltage name from V_{DD} to V_{CORE} Moved the Mailbox Interrupt Timing Diagram to be the final timing diagram Updated the Package Type for the CYD36S18V18 parts Updated the Package Type for the CYD36S18V18 parts Updated the Package Type for the CYD18S18V18 parts Updated the Package Type for the CYD18S36V18 parts Included the Package Diagram for the 256-Ball FBGA (19 x 19 mm) BW256 Included an OE Controlled Write for Flow through Mode Switching Waveform Included a Read with Echo Clock Switching Waveform Updated Figure 5 and Figure 6 Updated Electrical Characteristics for $\overline{READY}$ V_{OH} and $\overline{READY}$ V Updated Electrical Characteristics for V_{OH} and V_{OL} for the -167 and -133 speeds Included a Unit column for Table 5 Removed Switching Characteristic t_{CA} from chart Included t_{OHZ} in Switching Waveform OE Controlled Write for Pipelined Mode Included t_{CKLZ2} in Waveform Read-to-Write-to-Read for Flow through Mode

Document History Page

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REV.	**ECN NO.**	**Submission Date**	**Orig. of Change**	**Description of Change**
*C	402238	SEE ECN	KGH	Updated AC Test Load and Waveforms Included FullFlex36 SDR 484-Ball BGA Pinout (Top View) Included FullFlex18 SDR 484-Ball BGA Pinout (Top View) Included Timing Parameter t_{CORDY}
*D	458131	SEE ECN	YDT	Changed ordering information with Pb-free part numbers Removed VC_SEL Added IO and core voltage adders Removed references to bin drop for LVTTL/2.5V LVCMOS and 1.5V core modes Updated Cin and Cout Updated ICC, ISB1, ISB2 and ISB3 tables Updated busy address read back timing diagram Added HTSL input waveform Removed HSTL (AC) from DC tables Added 484-ball 27 mmx27 mmx2.33 mm PBGA package
*E	470031	SEE ECN	YDT	Changed VOL of 1.8V LVCMOS to 0.45V Updated tRSF VREF is DNU when HSTL is not used Formatted pin description table Changed VDDIO pins for 36M x 36 and 36M x 18 pinouts Changed 36Mx72 JTAG IDCODE
*F	500001	SEE ECN	YDT	DLL Change, added Clock Input Cycle to Cycle Jitter Modified DLL description Changed Input Capacitance Table Changed tCCS number Added note 31
*G	627539	SEE ECN	QSL	change all NC to DNU corrected switching waveform for (CQEN = High) from both Pipeline and Flow through mode to only pipeline mode Modified master reset description Modified switching characteristics tables, extracted signals effected by the DLL into one table and combine all other signals into one table updated package name Added footnote for tHD, tHAC and tSAC changed note 26 description

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REV.	**ECN NO.**	**Submission Date**	**Orig. of Change**	**Description of Change**
*H	2505003	See ECN	VKN/ AESA	Modified footnote #1 Removed 250 MHz speed bin Added 2-Mbit part and it's related information Changed ball name ZQ1 to DNU for 18M and lesser density devices Added 256-Ball (17 x 17 mm) BGA package for 18M Made PORTSTD[1:0] left and right pins driven only by LVTTL reference level For 1.8V LVCMOS level, Changed $V_{IH(min)}$ from 1.26V to 0.65 times V_{DDIO} and Changed $V_{IL(max)}$ from 0.36V to 0.35 times V_{DDIO} Changed tHD, tHAC specs for 36M from 0.6 ns/0.7 ns to 0.8 ns (See footnote# 32) Updated Ordering Information table

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